ECE 113B Final Exam

March 22, 2002
(Professor Kleinfelder)

CLOSED BOOK AND NOTES

To receive credit, please show all work and place your answers where requested.

NAME:_____ID:_____

Signature:_____Seat/Row:_____

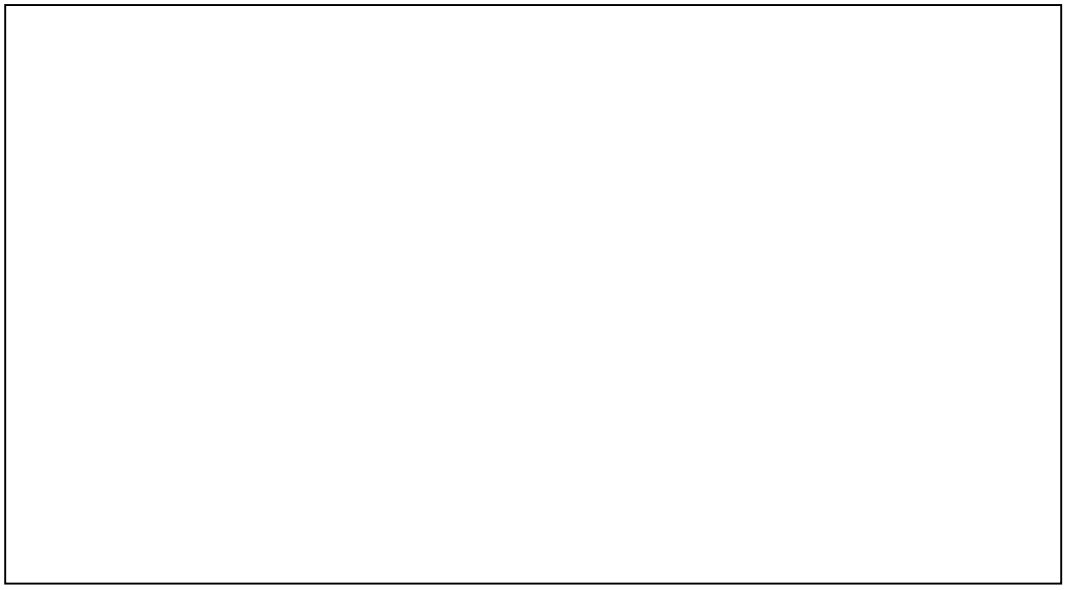
(2 pts) What is the *essential* design requirement for all *static* CMOS circuits?

_____

(2 pts) What would the main problem be with making an 8-input CMOS NOR gate?

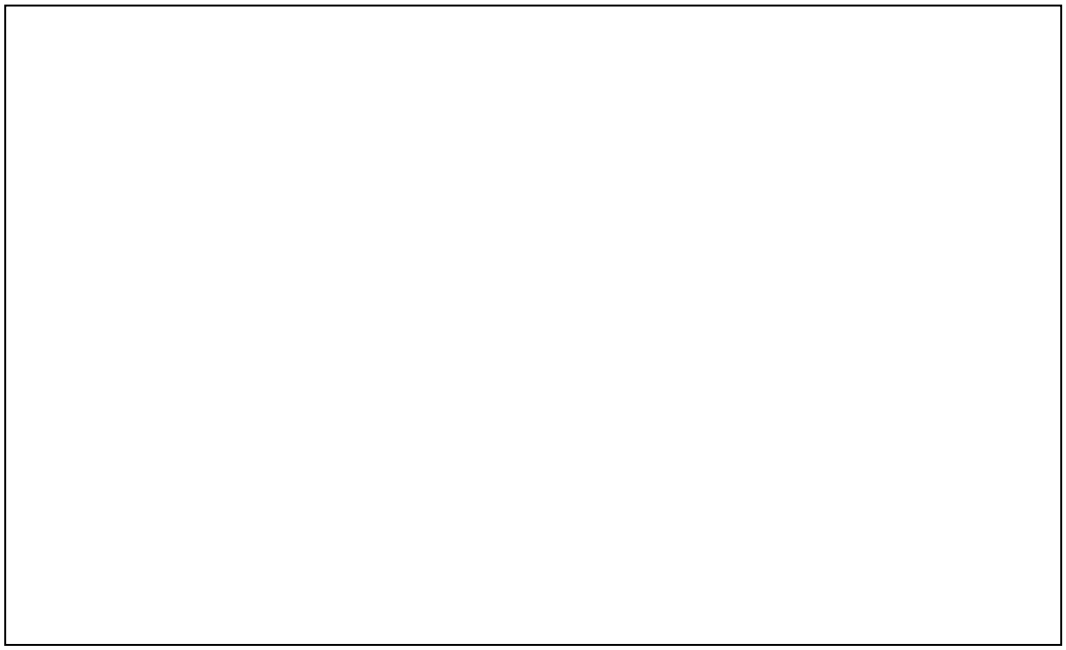
_____

(2 pts) Draw and label a pseudo-NMOS 2-input NOR gate:



(2) What essential condition must a designer guarantee for the above design?

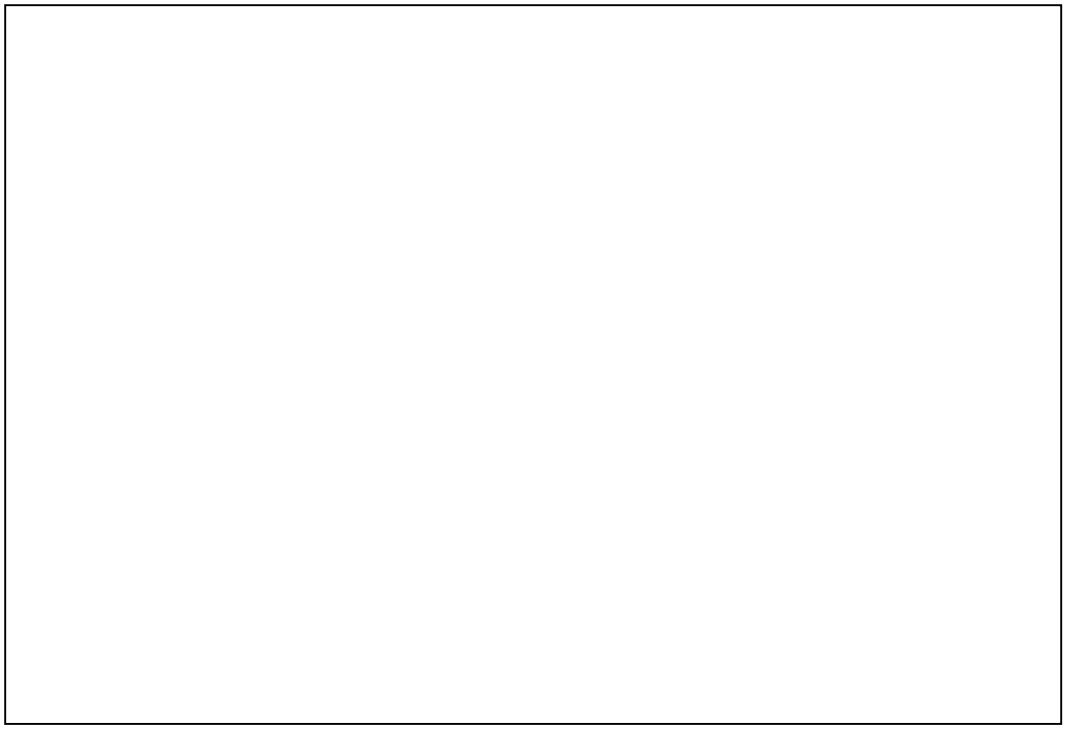
(2 pts) Draw and label a conventional dynamic 2-input NAND gate:



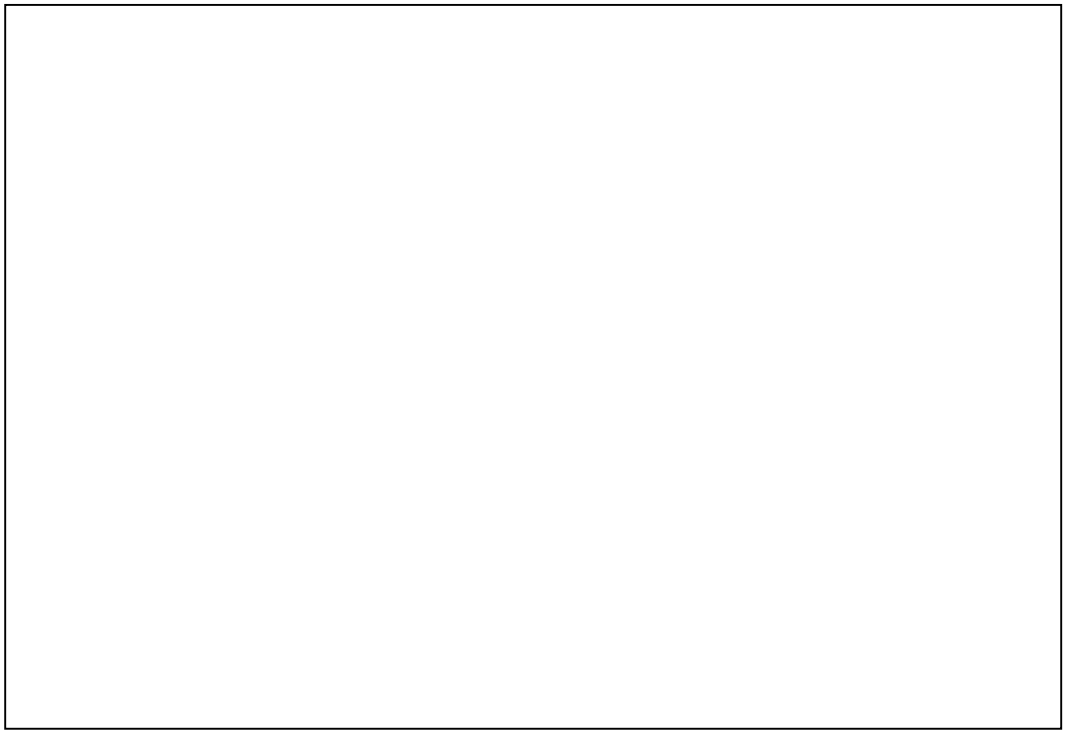
(2 pts) Explain what the “charge sharing” concern is in the above circuit:

(2 pts) Explain why cascading several of the above gates a bad idea:

(4 pts) Draw and label a dynamic 2-input NAND gate using a “keeper” transistor circuit that has zero DC power consumption. Label the inputs and the output:

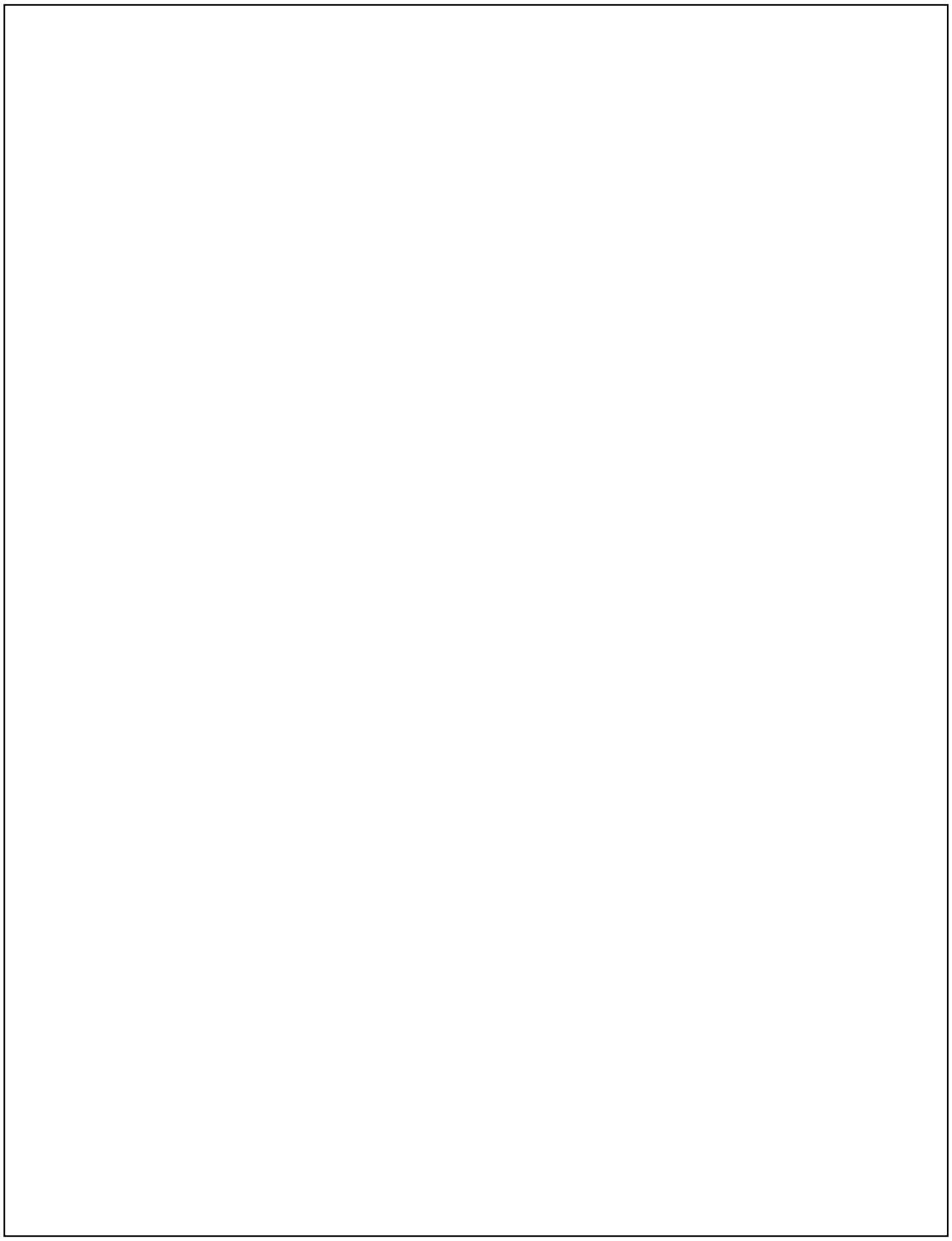


(4 pts) Draw and label a Domino 2-input NOR followed by a Domino 2-input NAND:

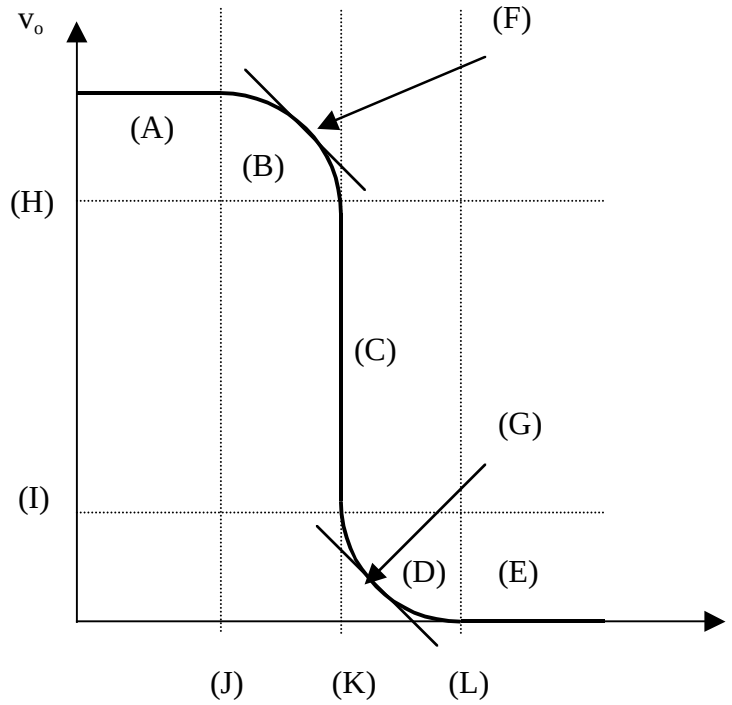


(10 points): Design a standard static CMOS circuit diagram of the following function, including worst-case W/L ratios using the method we studied in class. Use $\mu_n=2\mu_p$. You may wish to first draw it on the back and then copy it here when satisfied.

$\overline{Y=(A+B)(C(D+E)+FG)}$



The following shows the output transfer characteristic of a CMOS inverter, where the transistors are matched. $|V_t|$ for both transistors is 1V and Vdd=5V. Assume that the regions and lines shown are appropriate for the transitions and/or areas of interest as given in the book and lectures.



What mode of operation is each transistor in for each region (1 pt for each *region*):

	n-channel	**p-channel**
Region (A)	_____	_____
Region (B)	_____	_____
Region (C)	_____	_____
Region (D)	_____	_____
Region (E)	_____	_____

(1 pt each) Find the following voltages:

Voltage (H):_____

Voltage (I):_____

Voltage (J):_____

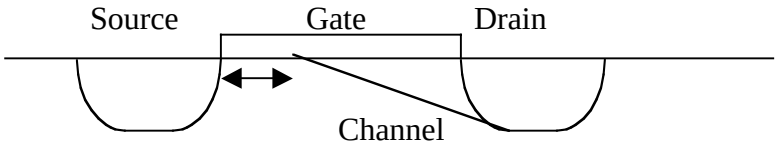
Voltage (K):_____

Voltage (L):_____

(1 pt) What are points (F) and (G) defined as?

Answer: _____

(2 pts) Write the equation for the drain current for the following transistor (side view), taking into account the phenomena that occurs when the arrowed line widens or shortens:

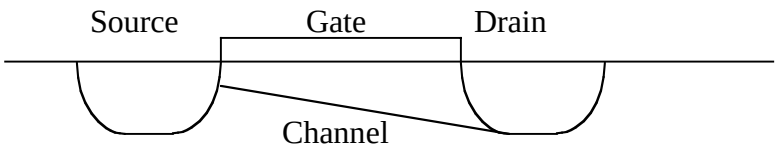


Answer:_____

(2 pts) If the above arrowed line widens or shortens, what is this phenomena called?

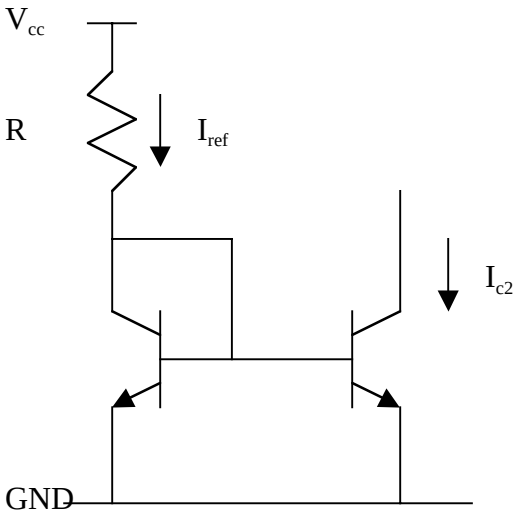
Answer:_____

(2 pts) Write the equation for the drain current for the following transistor (side view):



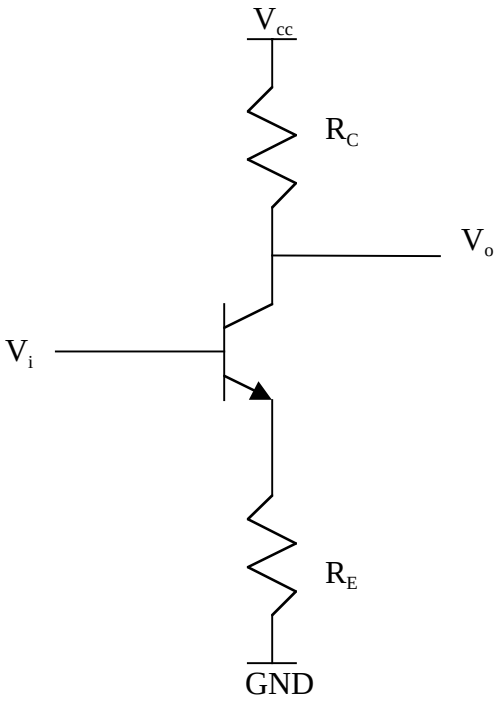
Answer:_____

(5 pts) Below is an NPN current source. The transistors are identical. Find I_{c2} as a function of I_{ref} and Beta.



Answer: _____

The following circuit is a common-emitter amplifier with emitter-degeneration, using simplified biasing. Remember that a voltage source denoted as V_i (capital and lower case) means a combined DC and small-signal source.



(5 pts) Draw the small signal equivalent circuit model for this amplifier:

(5 pts) Showing your work, what is the input resistance of this circuit?

Answer: _____

(10 pts) Showing your work, what is the transconductance of this amplifier? Reminder: The transconductance of an amplifier is $G_m=i_c/v_i$

Answer: _____

(2 pts) You are designing a 4096-bit dynamic RAM that has 8 parallel I/O bits. The memory array is square. Hints for these questions: Don't forget that the RAM has 8 parallel I/O lines. Also, the square root of 4096 is 64. First, how many address bits do you need for the word lines? Show your work or explanation.

(2 pts) For the above memory, how many address bits are needed for the column decoder? Show your work or explanation.

(4 pts) Draw a tree decoder for with two address bits. For the above memory, how many transistors would be needed to do the column decoding if you were using a pass-transistor tree-decoder architecture. Show your work and any explanations.

Answer: _____

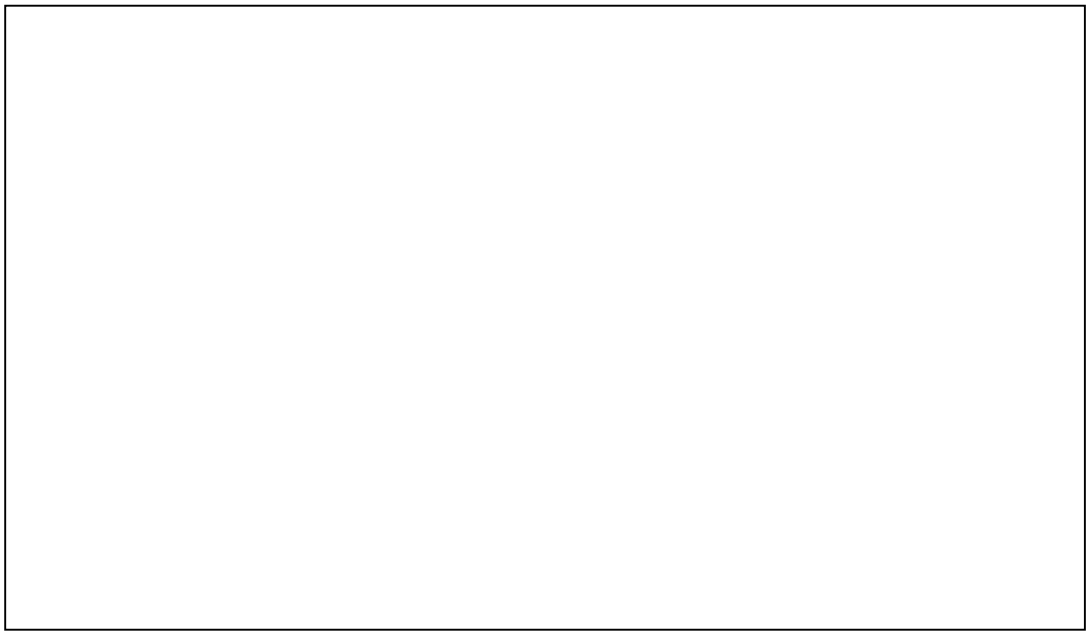
(8 pts) You want to make a "binary to gray code converter" and you have decided to use a read-only memory to do this. Below is a truth table that shows this conversion. Design a ROM that will do this conversion. You may use static pull-up transistors and, because it is so small, you can just use a simple inverter as a "sense amp." You do not have to design the decoder – you can just show a box with address inputs and *clearly* labeled word line outputs. Be sure to get the address correspondence and the polarity of the outputs correct. Again, you may wish to do this on the back and then transfer it here.

Input code (A3, A2, A1)	Output code (B3, B2, B1)
000	000
001	001
010	011
011	010
100	110
101	111
110	101
111	100

(4 pts) The resistance of an n-MOS pass transistor, as used in a tree decoder, for example, is an important criteria. Give a formula for the resistance of an n-MOS pass transistor when its source to drain voltage is small. Note that it would be in the triode region.

Answer: _____

(2 pts) Draw and fully label a conventional static RAM cell:



(4 pts) Suppose a dynamic ram cell with a storage capacitance of 0.1 pf, storing 0V, is read out onto a bit line with 10 pf capacitance that is precharged to 2.5 volts. What approximate voltage would the bit line initially settle to, prior to being driven by a sense-amp? Provide a formula or explanation.

Answer: _____

*** Extra Credit Problem ***
(10 extra points)

Suppose you wanted to use a CMOS inverter as an amplifier, biased at its switching point (you can assume that the two transistors are symmetrical). Draw the inverter with a reasonable biasing scheme, the small-signal equivalent circuit model of the amplifier and, showing your work, solve for the gain of the amplifier.

Gain: _____