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Building better buffers

Although an effective symmetrical buffer can be built from slow bipolar junction output transistors, D.Danyuk and G.Pilko suggest ways of improving performance in a conventional circuit.

The unity-gain buffer forms the building block of many analogue electronic circuits. To the best of the authors' knowledge it was first commercially employed by Harris Semiconductor in *HA-2600* op-amp[1] as an output stage. Several National Semiconductor products - Bi-FET op-amp *LH4104* with short settling time and unity buffer IC *LH0002* - might serve as more recent examples. This buffer is at the heart of the latest current-feedback op-amps.

The unity-gain buffer shown in **Fig.1** consists of a two symmetrical halves. Each of them is an emitter follower with opposite polarity transistors, connected in series. Each half and the complete circuit have nearly zero dc offset voltage. The bases of input followers are connected together without any biasing network. The buffer input resistance is comparatively high, which, taken in conjunction with a low output impedance, leads to a high degree of isolation between input and output buffer nodes.

The emitter currents of input followers are set by current sources. The voltage drop on the input transistors' emitter junctions and R_1, R_2 serves as a bias voltage for output followers. A local current feedback through R_3, R_4 gives acceptable temperature stability of output transistors' quiescent current.

Two difficulties are inherent; the first is a low load capability. An output-transistor base current is limited by the value supplied by the current source, and the maximum output voltage (**Fig 2b**) can be expressed by:

$$V_{out}\max = I_{out}\max R_L = \left(h_{FQ_3}+1\right) I R_L \quad ..1$$

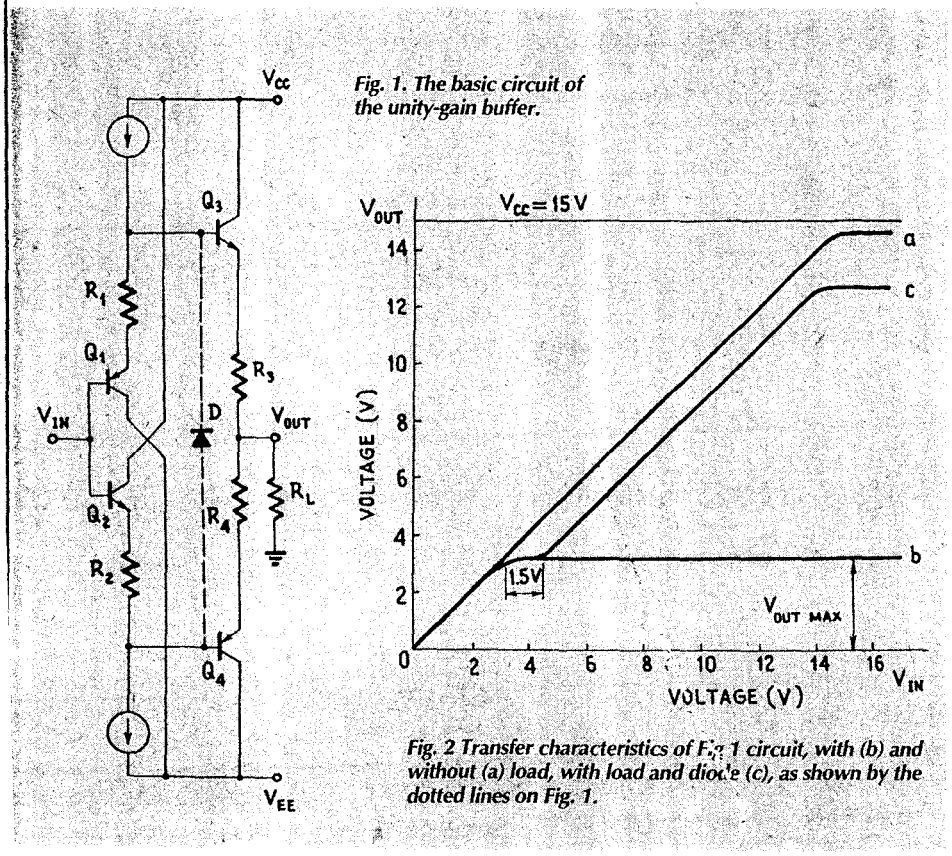


Fig. 1. The basic circuit of the unity-gain buffer.

Fig. 2 Transfer characteristics of Fig. 1 circuit, with (b) and without (a) load, with load and diode (c), as shown by the dotted lines on Fig. 1.

where I_{out} max is the maximum output current, h_{FQ3} is an output transistor (Q_3) dc current gain, I is the output current of a current source, R_L is a load resistivity. If the current sources are replaced with resistors R, equation [1] will be:

$$V_{out}\max = V_{cc} R_L \left(h_{FQ_3}+1\right) / \left(R + R_L\left(h_{FQ_3}+1\right)\right) \quad ..2$$

where V_{cc} is a supply voltage.

The second problem is that the buffer input followers drive capacitive loads – the output transistors' collector to-base junction capacities. The voltage step with small rise-time comes at the input, one of the input transistors cuts off and the output transistor collector-to-base capacitance charges slowly through the current source. This leads to slew-rate limiting and is shown clearly in **Fig. 3**. The output pulse edge breaks in two parts, when one output transistor turns off quickly and another turns on slowly. The output waveform becomes much worse with capacitive loads.

One of the simple methods is the diode placement between output transistor bases, as shown by dotted lines in Fig. 1. In this way a new path for an output transistor base current is open and base current value is no more restricted. The corresponding transfer characteristic Fig. 2c contains a pair of 1.5V dead zones. These features are hardly removed by feedback and cause a large amount of distortion.

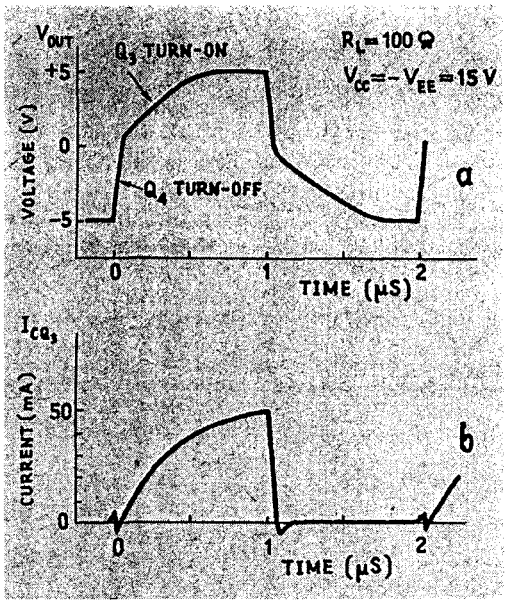


Fig.3 Transient responses of Fig 1 circuit driving a 50Ω load, output voltage (a) and Q^3 collector-current (b). Current sources are replaced with 5.1kΩ resistors.

Darlington-connected output stage

It is possible to improve the buffer performance by a more straightforward approach: increasing the output stage current gain. The possible circuit arrangements of Darlington-connected output transistors are shown in **Fig 4**.

Fig.4 The unity-gain buffer with Darlington-connected output transistors, with different paths for driver transistors (Q5, Q6) emitter current flow.

It is well known that if higher frequencies are fed into a push-pull output stage, the output transistors will both be partly on for a considerable portion of each cycle. This is like connecting the positive to negative supply by turning on both output transistors. The extra current conduction is referred to as 'mutual' or 'common-mode' conduction. The storage time effect in output transistors causes secondary crossover distortion, reduces high-frequency power efficiency and increases high-frequency distortion.

Three structures (Fig. 4) were tested for susceptibility to 'common-mode' conduction. One of them is an ordinary configuration with base-bleeder resistors (Fig 4b). Two others are without direct connection between output and driver transistor (Q_5, Q_6) emitters. The circuit shown in Fig 4a was offered by B N Locanthi[2] and the circuit shown in Fig 4c by J.M.Diamond[3]. Driver transistor quiescent currents were set equal for all configurations.

While it seems that available turn-off output transistor base-current is limited to the amount of a driver transistor quiescent current, the circuits shown in Fig.4 present a somewhat different performance.

The idle peak current values amounted to 100% of an output current with square-wave input. A typical collector current waveform for an output transistor is shown in **Fig. 6a**. The falling edge of an output transistor collector current for the circuit Fig.4a was one and a half times shorter than for the ordinary circuit (Fig. 4b) and twice as short as the circuit in Fig 4c.

This occurs for two reasons. First, each base of the Fig.4a output transistors has a low-resistance path for the reverse base current to flow

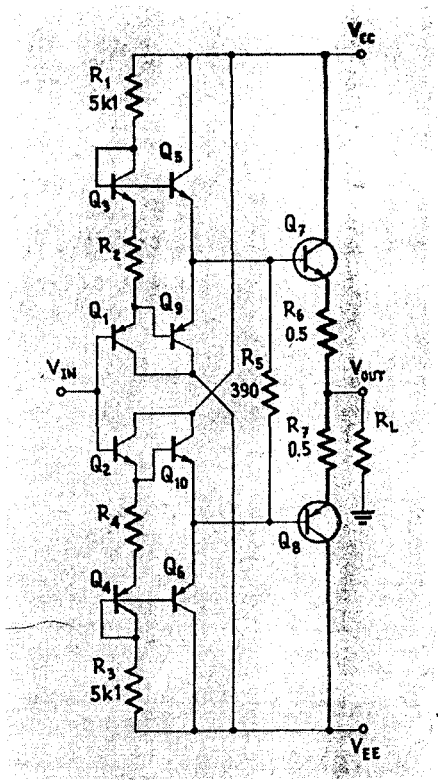
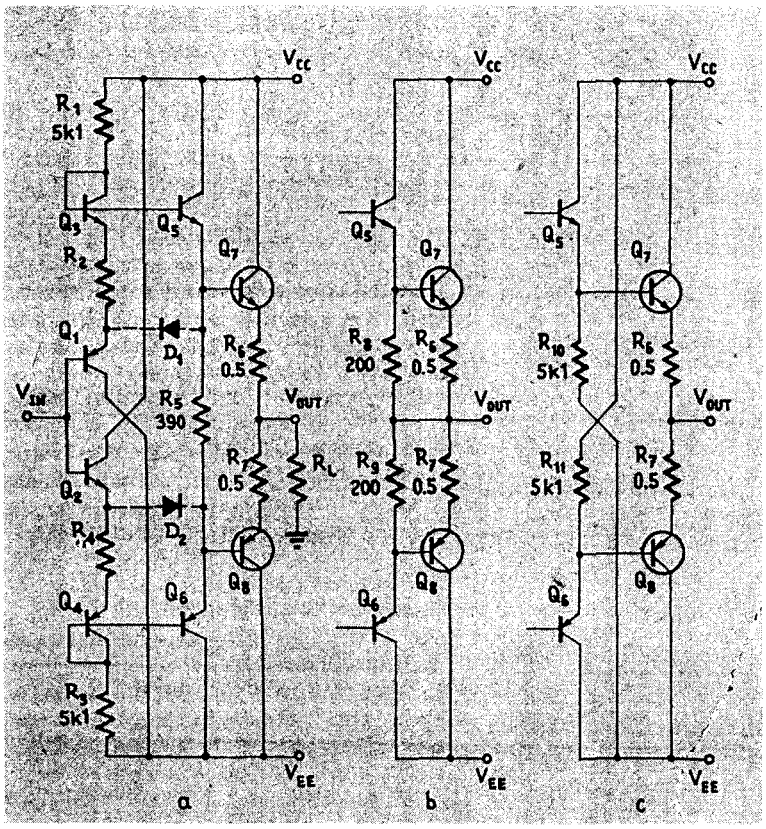
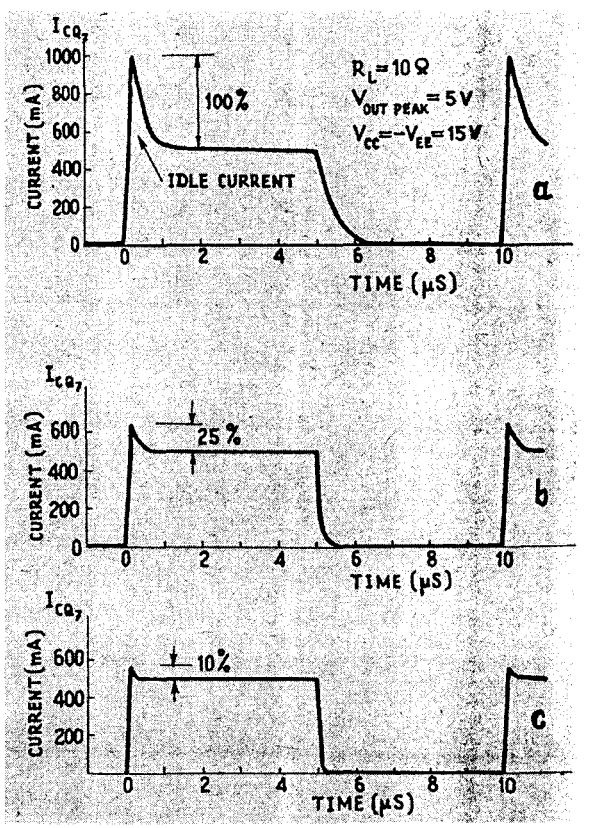


Fig. 5. Improved version of Fig. 4a circuit with additional emitter followers (Q_9, Q_{10}) for fast output transistor turn-off.

Fig. 6. Transient responses of Fig. 4, 5 circuits, n-p-n output transistor collector current for Darlington-connected version Fig. 4a (a), for Fig. 4a with diodes D_1, D_2 (b), for Fig. 5 circuit (c).





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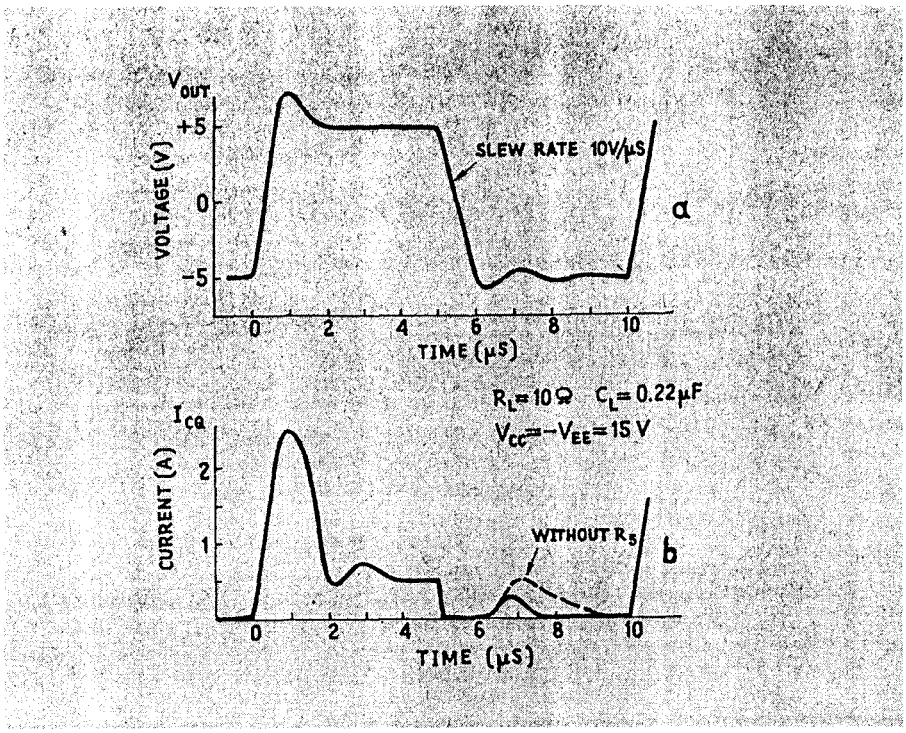


Fig. 7 Transient responses of Fig. 5 circuit driving a 10Ω load with 0.22μF in parallel, output voltage (a) and Q_7 collector current (b). Lower graph shows the effect of R_5 moving.

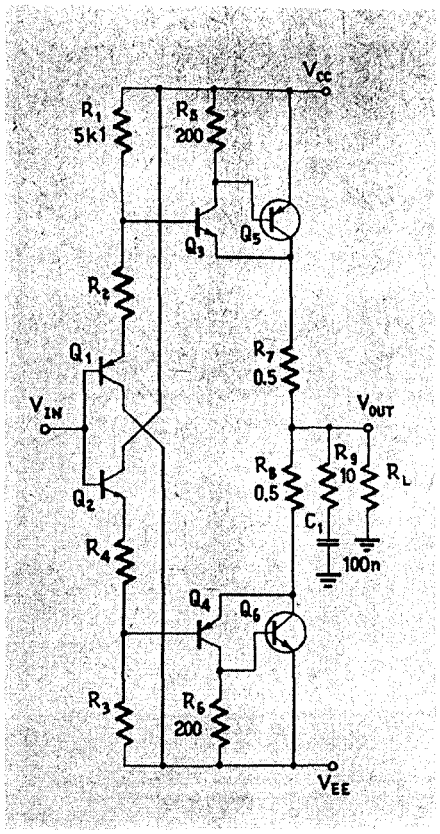
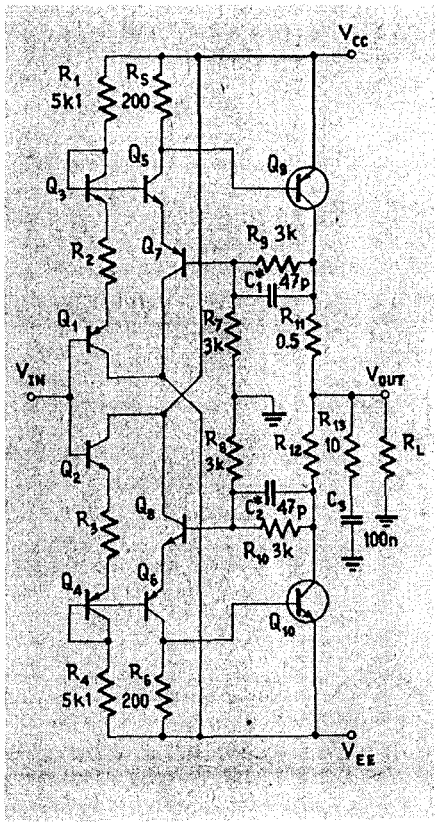


Fig. 8 The unity-gain buffer with a complementary compound output stage.

Fig. 9 The output stage with improved thermal stability. Output transistors are driven with complementary versions of a balanced common-emitter stage.



through its opposite emitter driver stage. Second, the driver transistors never cut off under load.

For high-speed transistor operation one should make use of L Hart's idea[4] and drive an n-p-n transistor from a current source with a special waveform. It envisages a positive spike for fast turn-on and a negative spike for fast turn-off as its components. Driving the output transistor from the low-impedance point gives nearly the same base current waveform and decreases the idle current to a negligible value. This can be realised by inserting the additional diodes D_1 D_2 as shown by dotted lines in Fig.4a or emitter followers Q_9, Q_{10} (**Fig 5**).

The low impedance aids in draining out the charge stored in the base region of the output transistors, thus speeding up their turn-off . The output square wave rise-time is improved by a factor factor of two, from 70 to 40ns. It should be noted that the first configuration (Fig. 4a, with D_1, D_2) operates satisfactorily with low and medium impedance input signal source only. **Figure 6** illustrates the output transistor collector current waveform for several of the topologies listed above.

A decrease in the output device turn-off time also gives an important improvement in effective safe operating area. The safe area of an output transistor is a region that is restricted by voltage, current, time and temperature limits which the device would stand without damage. The absolute current limit is set at low voltage by the fusing characteristics of the bonding wire, so the current spike after transistor turn-on should be considered.

At the falling edge of the collector current waveform, the device operates with rather high collector voltages near (or beyond) a secondary breakdown region. When an ordinary output stage operates with high capacitive loads, the falling edge of extra collector current is stretched in time, and the operating levels may exceed power dissipation and secondary breakdown boundaries.

Figure 7 shows the rather high load capability of the Fig 5 circuit. The output transistor collector current waveform (Fig 7b) is almost free from 'common-mode' conduction and has a sharp turn-off edge. R_5 helps to decrease the turn-off current residue. With a capacitive load an output follower has a negative input conductance that decreases with the transition frequency of the output device. These elements, with the output follower collector-to-base capacitance, form a parallel resonant circuit which causes peaking in the output waveform.

Compound output stage

The complementary compound output stage (**Fig. 8**) seems to be another solution to the increase in the output stage current gain. The circuit has a greater thermal stability due to the existence of current feedback loops. These loops contain Q_3, Q_5, R_7 and Q_4, Q_5, R_8 and the loop gain value can be expressed by:

$$\beta A = 26mV R_7 h_{FQ_5} / I_{EQ_3} \qquad ..3$$

where 26mV / I_{EQ3} is a driver transistor (Q_3) transconductance and h_{FQ5} is an output transistor (Q_5) dc current gain.

It appears to be convenient to have some gain in an output buffer to provide nearly a full output swing.

The presence of a feedback divider in the driver transistor emitter network decreases

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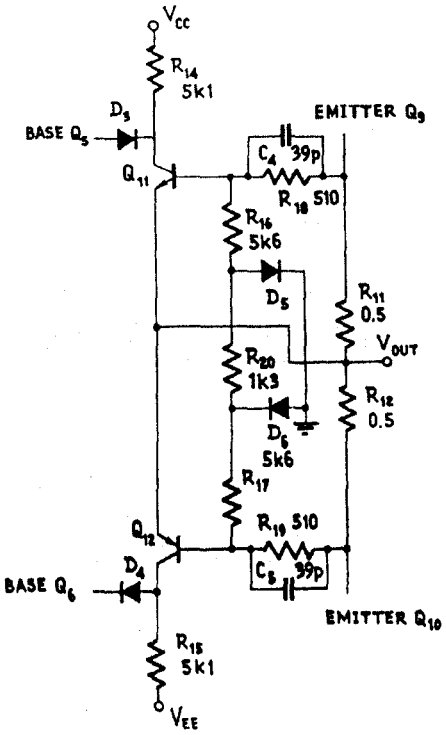

Fig. 10. Suitable overload protection circuit with SOA control.

current loop gain βA to:

$$\beta A = \beta R_F h_{fe_{Q_5}} / R_f \quad ..4$$

where β is a feedback divider attenuation ratio and R_F is a feedback network output resistance. A feedback network output resistance serves as a local feedback element. Current loop gain is decreased mainly due to driver transistor transconductance reduction by a local feedback and current loop gain βA is far lower than unity. Thus, the compound stage thermal stability becomes equal to a Darlington connected one.

One of the options for restoring current feedback loop gain and maintaining the thermal stability was employed by E M .Cherry[5]. In his circuit, the output transistors were driven by a pair of differential amplifier stages. An alternative solution is shown in **Fig 9.** The complementary versions of a balanced common emitter stage gives the same current loop gain value but eliminates a slew-rate limiting effects. These effects occur when the output transistor collector-to-base capacitance charges from the long-tail pair current source.

The modification is not that simple: a compound output stage is used to fasten the output transistors' turn-off at this stage. An output transistor collector current waveform is similar to the one shown in Fig. 6a, with the falling edge time interval one and a half times longer.

In the designs of Figs. 8 and 9, the 10Ω and 100nF Zobel network prevents the effective load from becoming too high and provides adequate stability in the feedback loop.

Figure 10 illustrates a suitable overload protection circuit with safe-operating area control. This circuit should be used with any of the configurations listed above.

Realisation

The circuits shown in Figs. 1-9 were realised with a pair of quad-transistor arrays and *BD233/BD234* output devices. Several units were manufactured in a hybrid IC form. Output transistor bias currents were set in the range of 10 to 30mA by the proper choice of the input follower emitter resistors. Their values varied from zero to 10Ω due to U_{BE} mismatching.

The paper discusses the practice of realising a symmetrical buffer topology using rathe slow bipolar junction output transistors. The above analysis suggests some additional measures for improvement in a conventional circuit (Fig.1). The circuit shown in Fig. 5 would give the best performance in terms of speed and 'common-mode' conduction and seems to be suitable for high-speed operation with complex loads. The circuit shown in Fig. 9 is expected to give both higher linearity and thermal stability and appears to be acceptable for use with slower op-amps.

In passing, it should be noted that the results obtained are applicable to various output stages irrespective of power level or biasing network configuration. ■

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BOOK REVIEW

Fibre Optic Cabling, by Mike Gilmore, extends the understanding of optical fibres needed for practical application in telecommunications and data-comms to a more soundly based level, at which theory can confidently be applied to unfamiliar techniques. Nonetheless, this is essentially a practical treatment for engineers and laymen alike, which also covers the installation and commercial aspects of the technology.

Optical fibres in general terms and their use in communications form an initial chapter, as an introduction to more specific discussion. Five chapters cover fibres and connection practice, both theoretical and practical considerations being treated, and are followed by three more on cables, highways in general and design in particular. A final chapter on the hardware of optical fibres then presents the choices available in cables and assemblies, connectors, splicing and enclosures.

Specifying fibre systems appears to be an undeveloped art, its vagueness contrasting sharply with that commonly found in copper cabled systems; one chapter is therefore an attempt to introduce a little rigour into the process.

Acceptance testing, installation practice and final acceptance testing are all subject to contractual obligations and are therefore supremely important if reputations are to survive a contract; three chapters describe methods of ensuring survival of both reputations and systems. Documentation and maintenance form the two final chapters in the design and installation part of the book, but the penultimate section is illustrative of the author's experience with real systems — a case study. Future developments such as single-mode fibres and fixed, blown-fibre cables are then discussed in an end-piece.

This is no "penny-a-line" text cobbled together by a media man, but is the result of hard-won experience by a practitioner, the author not only being Managing Director of an optical-fibre cabling company, but also chairman of one of the BSI working groups in this area.

Butterworth Heinemann, 318 pp, hardback, £35. H M Howarth is the third volume in the Chapman and Hall series "Physics and its Applications", some of which are said to be suitable for final year degree courses and postgraduate work, although this particular one seems to be intended for slightly earlier work.

Widely used theorems are treated - Thevenin, Norton, Millman –and the book begins in a fairly peaceful way by covering DC and AC current theory, j notation and the complex-frequency s notation.

Mesh and nodal analysis take up a chapter before the foregoing is used to explain the network theorems from Thevenin to star delta, by way of superposition and reciprocity. Resonance and coupled circuits each have a chapter and the final section is on two-port networks, including transmission lines and artificial delay lines.

No great mathematical demands are made on the reader, who should find that simple calculus and a familiarity with matrices will be enough. This is a dead-pan, straightforward book, with no attempt at lightening the subject and, as such, is a workmanlike production. I saw no "It can be shown ..."s.

Chapman and Hall, 160 pages, paperback, £11.95.