ICON

The cadence Newsletter

November 2002

CONTENTS

November marks the onset of winter around the country, with weekends and holidays typically spent indoors with family and friends. It also gives one the opportunity to catch up on reading, and the November ICON brings you some great material to drive the winter blues away! This issue carries two articles, one on SoC Verification, and the other on Wireless Communication, authored by experts on these topics at Sasken Communication Technologies Limited. Sasken is a leading design services company in India, with a focus on the telecom sector. These articles represent the individual expertise of the authors as well as the institutional knowledge that resides in Sasken.

On another note, November also marks the final issue of the 2002 ICON series. With the editorial team taking a short break, on behalf of all of us here at Cadence India, I would like to wish you a very happy new year in advance, we'll see you in January 2003!

Regards
Rohit Biddappa
Editor

The Cadence Bangalore family expands once again, with Mohan Kamaraj joining the team as a Senior Application Engineer. Mohan has spent over four years in VLSI design, with experience in logic design, synthesis, verification, design for test, and also brings with him valuable domain knowledge covering FPGA and board level design. Apart from the above, in previous jobs, Mohan focused on Verilog and VHDL for RTL synthesis and verification, where he built extensive experience in digital design. In his present capacity at Cadence, Mohan is tasked with supporting the entire Verification Acceleration (earlier known as Quickturn) range of products, including the Palladium hardware emulator. Mohan's biggest passions are cricket and music, which helps him relax and unwind.

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3C's IN AN SOC VERIFICATION

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Abstract: The complexity of present day System-on-Chip (SOC) is increasing tremendously with more and more components (IP's) being put on a single piece of silicon. As the size of the designs double their verification efforts quadruple. It may be relatively easy today to design an IP or module, but to integrate it correctly in an SOC is challenging. In other words, to verify a design in a complete system perspective is really demanding. Although, the individual components are rigorously verified, the main focus in SOC verification is on checking the correct integration between the various components. This task becomes more difficult since many IP's are from different vendors and may not have desired or well-defined interfaces for a particular application.

This paper discusses the verification of present day SOC's built using different IP's. It defines the verification efforts under 3C's namely, Connectivity, Controllability and Coverage. These terms have been explained in detail. The 3C model has been defined as a heuristic relation to correlate the 3C's. Finally the paper touches upon post-synthesis verification efforts and their usefulness.

1. INTRODUCTION

The revolution in fabrication technology has enabled integration of hitherto discrete system components on to a single piece of silicon forming present day System-on-Chip (SOC).

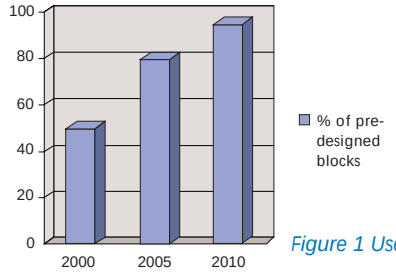

Figure 1 Use of Pre-designed blocks

The time to market constraint and availability of many such discrete components as an individual product or IP in the market has considerably reduced the turn around time of an SOC. It is now possible to build an SOC by simply integrating various IP's without even designing a single block. The success of designs in coming days will depend to a great extent on the availability of pre-designed blocks. It consumes lot of time and is impractical to design all the blocks in an SOC, afresh. The importance of pre-designed blocks can be seen from Figure 1, which shows the estimated % usage of pre-designed blocks with respect to time. As indicated in the figure, by the year *2005, 80% pre-designed components* will get used in an SOC.

With the advent of IP's, design of an SOC is easy but its verification is increasingly becoming more complex. Almost 50-70% of time and resources is consumed in only verifying a design [3]. The verification therefore needs to be more organized, efficient and easily measurable with a suitable metric.

The IP's received from various vendors are sometimes required to be customized for the targeted application. This may require changes in IP or its interfaces. It may be a complex process and requires a lot of knowledge about the IP. The IP then need to work correctly in the system. The key challenge in SOC verification is therefore the correct integration of these IP's. This will be the main task, as more and more pre-designed components will get used in future as can be seen from the data in Figure 1.

The efforts spent in verifying an SOC design can be broadly placed under 3C's that dominate the complete verification. These C's are: Connectivity, Controllability and Coverage. They can be effectively placed under single word, *Correct Integration*. Algorithms can be developed around these C's to quantify the index of verification.

The complexity associated with an SOC verification demands very stable and consistent verification environment. It also requires faster simulators and higher degrees of automation. It would be impractical to do the verification manually.

An IP can be used in different types of SOC's. This suggests that the verification components can also be reused with minor changes. These days great amount of effort is spent to create a verification environment that can be easily reused. The verification IP's are therefore in high demand to ease the increasingly complex SOC verification. There are methodologies like eRM (e Reuse Methodology, [2]) to enhance the reusability [4].

The software is a vital component of an SOC. The correct working of an SOC is guaranteed only if Hardware and Software are correctly integrated. We therefore need to verify both of them together as complete system components. This suggests application of methods like Hardware-Software co-verification where software component of an SOC is run on the simulated hardware. This is known as Virtual Prototyping [5].

This paper describes the 3C's in detail and their usefulness in SOC verification. The 3C model is also proposed as a heuristic correlating the 3C's. We also describe in brief about the efforts spent in post-synthesis verifications and their usefulness.

2. 3C's IN AN SOC VERIFICATION

While doing SOC verification it is explicitly assumed that individual IP's or modules are verified rigorously and are bug free. The main

concern is correct working of them in a complete system.

3C's namely correct Connectivity, Controllability and Coverage primarily dominate the verification of an SOC. Although, there are lots of activities that happen in verification and in fact it is difficult to decide the limits for verification, still, we can club the verification activities in 3C's and correlate them with 3C model. Let us examine each component in detail.

Connectivity

We define *Connectivity* as the ability of an IP to correctly communicate with another IP of an SOC. In other words, if it can fulfill all the handshaking/protocols required for communication and is able to transmit and receive the data, then we say that it has correct connectivity with that IP. It, therefore, means that IP's are working correct, functionally. For example, if an IP wants to transfer data to another IP and it completes the protocol required for this, like correct sequence of request generation, direction of transfer, number of bytes to be exchanged and acknowledgement from the other IP, then, we say that IP has correct connectivity with the accessed IP. In other words, if it is able to exchange the data following the correct protocol, then, we have verified its connectivity. Like this we have to verify the connectivity of an IP with all other IP's with which it can communicate. When all such connections are correct then we can say that an IP has correct connectivity in SOC.

If the communication between two IP's is via a third IP (e.g. bridges) then the correct communication between two end IP's will verify correct connectivity of intermediate IP's. We can also verify the connectivity from source to intermediate IP and from intermediate to destination IP. Similarly, if interrupt is an event to confirm a particular operation, then, correct issue of interrupt can be verified if the processor serves the corresponding ISR (Interrupt Service Routine).

Controllability

The second C of our 3C model is the *Controllability*. We define the controllability as the ability of a master IP to have a complete control or command over its slave IP. In other words, if the master expects slave to behave in a particular manner then it should be able to do so. The major task here is to verify if a master can configure the slave environment as per its requirement. This mainly involves configuring and accessing the slave registers. Therefore, here the controllability is concerned with the programming of the registers only and the protocol adherence is taken care in connectivity.

In order to verify the controllability we need to write into the slave registers and read from them. This task may be tedious, as the numbers of registers to be accessed are very large. For example, the processor acts as a master for many IP's and we actually have to write/read in those registers to verify its mastership. Also, all the bits of registers may not be writable and they also need to be verified for the same. This will require a different mask pattern for each register.

In a typical verification scenario of an SOC lots of test cases are written to verify controllability. Although, the number of test cases to verify the connectivity outweighs the test cases for controllability, still verification is generally started with the latter ones, as it is easy to verify them. It gives a good confidence of the working of our verification environment. We have to verify the reset values of registers also along with their normal write/read values.

Coverage

The third C of our 3C model is the *Coverage*. One of the significant requirements of a good verification is a correct metric to indicate the progress and effectiveness of verification. Coverage is one such metric. It can be divided into two components: code coverage and functional coverage. The code coverage only indicates which lines of the design codes are executed and do not give explicit indication about features of the design covered. Therefore, these days great amount of emphasis is given to functional coverage. In this paper coverage refers to functional coverage only.

We can define functional coverage or coverage as the effectiveness of test cases to cover the features in complete design space. In other words, it indicates the extent to which test cases have covered the features defined in the design specifications. The coverage will not only indicate test base effectiveness but will also help in writing new test cases to hit the uncovered design features. Coverage is a goal as well as metric.

In order to calculate the coverage we need to define monitors. They will actually indicate if a particular feature is covered by test cases. There can be a monitor for each feature of the design or a single monitor may cover multiple features. This can be done either manually or with the help of a tool. We have to first define the exhaustive set of monitors for all the features to be covered and then find out how many monitors actually got hit by test cases. Let us say that we have defined monitors to cover N features of the design out of which F features got hit by test cases then we can use the following relation to calculate the coverage:

$$\text{Coverage (\%)} = (F/N) * 100 \qquad \ldots(1)$$

This is an important figure and generally should be more than 98% to have good confidence on verification efforts. It is always defined with reference to the total defined features, N. It, therefore, indicates that we have to write new test cases to cover the remaining (N - F) features. Coverage is clearly an explicit quantitative measure of verification.

3. THE 3C MODEL

In order to have effective SOC verification, we need to verify complete *data and control paths* meshing the entire system. The former will correspond to Connectivity and the latter to Controllability defined with reference to the features of the design. If we define C_{eij} as the connectivity of an i^{th} IP with j^{th} IP and C_{bij} as the ability of the i^{th} IP to control j^{th} IP, then, we have the following heuristic 3C model for feature coverage, C_o:

$$Co = C_{eij} + C_{bij} \qquad \ldots(2)$$

Where, n = total number of IP's in an SOC
i,j = positive integers from 1….. n (i „ j)
The summation is for all the n IP's over all i and j (i „ j)

The above relation is another quantitative way of visualizing verification. The relation is proposed with reference to the features of the design defined in specifications and that are required to be covered by test cases. C_{e12} is the connectivity of IP-1 with IP-2 and constitute one feature. C_{e21} is the connectivity of IP-2 with IP-1 and constitute another feature. C_{e12} may not be equal to C_{e21} depending upon the protocol and therefore, different monitors must verify both the features. Similarly, C_{b12} is the ability of IP-1 to control IP-2. The model is valid for one C_{eij} and C_{bij} feature between any two IP's and not for multiple features between the same IP's. It is therefore a good point to start with this model to have a coarse or first cut measure of verification.

The 3C model is an attempt to correlate the 3C's. In the above relation if i = j, then the corresponding C_{eij} and C_{bij} are not valid (they will be equal to zero) as they define connectivity and controllability of an IP with itself which is self-evident. Similarly, if there exist no connectivity between i^{th} and j^{th} IP i.e. they are isolated, then, their corresponding C_{eij} and C_{bij} are zero.

4. POST-SYNTHESIS VERIFICATION

The net-list verification will give a finer look to the design with respect to timing as well as functionality. The use of techniques like Formal verification and gate-level verification using hardware accelerator will be more accurate as they are based on net-list that is close to the actual silicon. The results from post-synthesis verification should augment and re-validate the observations at RTL level. There can be lots of verification iteration after RTL and net-list changes to re-validate the equivalence.

There can be many reasons to do the post-synthesis verification to validate the 3C's. The formal techniques will verify the functional correctness of system after changes are introduced in RTL or net-list. They are used for equivalence checking.

The Gate level verification using hardware accelerator will give extra confidence in the netlist. This is very time consuming and complex verification process and therefore only few tests are run where there is maximum activity happening in the complete system. The netlist is back annotated with SDF (Standard Delay Format) which is extracted from the post-layout netlist and therefore, time accurate.

The main challenge here is to initialize all the relevant signals and registers to avoid the propagation of "X" across the whole system as here we work with actual hardware components.

The Gate level simulation will verify the asynchronous signals timing also. The outputs of these simulations can be used to generate the test vectors for post-silicon functional validation. They, in conjunction with ATPG test vectors, will run on the actual silicon using testers. They will exactly verify the Connectivity, Controllability and give an indication of Coverage.

5. CONCLUSIONS

This paper analyzed the problems faced in today's SOC verification. It described the challenges that come in verifying an SOC assembled using IP's. In order to do effective verification we need to concentrate on 3C's in an SOC verification: Connectivity, Controllability and Coverage. These C's can be correlated with the 3C model to guide the verification efforts. The model was defined with reference to features of the design defined in specifications.

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5. Technical papers at www.mentor.com

Biography of Vishal:

Vishal has done his masters in VDTT (VLSI Design Tools and Technology) from IIT Delhi. He joined SASKEN as a campus recruit and has worked there since Feburary 2000. His master's thesis work entitled "Software Power Optimizations in an Embedded System" was published in the 14th International Conference on VLSI Design, 2001. At present he is involved in system level verification of a multi-million gate SOC. His interests lie in Front End Design and Verification of SOC especially in low power, high performance designs.

He is also interested in teaching and organising technical events and seminars.

Answers to ICON QUIZ – October 2002

Which feature in Cadence's Soc Encounter™ architecture enables designers to build module level floor plans that would automatically generate timing budgets and optimized pin assignments based on a full chip parasitic aware Timing Analysis ?

Ans: In-Context Partitioning

Winners of ICON QUIZ

Congratulations to the winners of ICON QUIZ – October 2002!

Mr. Dharmendra Lingaiah
Cranes Software International Limited
Bangalore

Mr. Gopi Krishna
QualCore Logic Ltd
Hyderabad

Mr. K Gopal
QualCore Logic Ltd
Hyderabad

OFDM BASED MIMO WIRELESS COMMUNICATION SYSTEM

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1. Introduction

The future mobile communication systems or the next generation (NG) wireless systems require newer value add in terms of applications, services, terminal features etc. from end-user perspective. While the NG specifications and features continue to be debated, the need for a new air interface technology that is capable of carrying broadband data with a high spectral efficiency is undisputed in order to maximize the scarce frequency spectrum resource. High spectral efficiency can be achieved by using innovative and adaptive modulation techniques, Multiple Transmit and Receive Antennas, Antenna Arrays etc. Orthogonal Frequency Division Multiplexing (OFDM) [1] modulation scheme offers efficient frequency usage and is well suited for broadband mobile applications. The Multiple-Input-Multiple-Output (MIMO) technology can be used to exploit the spatial diversity by the use of multiple antennas on both, transmit and receive sides. MIMO has been shown to achieve large spectral efficiencies, as high as 50 bit/sec/Hz as demonstrated by research prototype [2].

This article briefly describes the Orthogonal Frequency Division Multiplexing (OFDM) and MIMO technologies and an OFDM based broadband communication system using a 2x2 MIMO scheme. The Broadband Wireless Baseband Layer was designed and simulated using Cadence's Signal Processing Workbench (SPW) System Simulator.

1. Towards higher Spectral Efficiency

Need for higher and higher data rates and multiple applications with different quality of service requirements in the future will require technologies which are highly spectrally efficient and which can fight multipath effects well. Spectrally efficient modulation techniques, adaptive modulation, multiple antennas (MIMO) and array processing can give high spectral efficiency by increasing the channel capacity dramatically.

While CDMA and TDMA based technologies will fight for a place in this competition, it is expected that *OFDM technology* will meet such requirements better. OFDM is spectrally most efficient since the sub-carriers are overlapping.

Adaptive modulation can increase the data throughput by dynamic control of the data rates so as to minimize the fading effects of the multipath channel. The modulation can be changed to send low bit-rate with increased probability of being correctly received for instances of frequency or time fading while maximum possible data rate can be used under good channel conditions. This will result in improved channel capacity.

MIMO schemes with n transmitter antennas and m receiver antennas are shown to improve the channel capacity by at least a factor equal to the lower value of n, m. Space Time Coding techniques can be used to enhance the performance of MIMO systems which in addition to exploiting the spatial and temporal diversity offer additional coding gain.

Array processing is used to compute the received signals from multiple antennas. Array processing in some cases can also control the effective radiation pattern of the antenna array to maximize the received energy in certain direction(s) while minimizing it in the interference directions thereby increasing the cell capacity (Smart Antennas). However, the Smart Antennas are currently being researched primarily for base stations.

Figure 1 shows the block diagram of a MIMO wireless system.

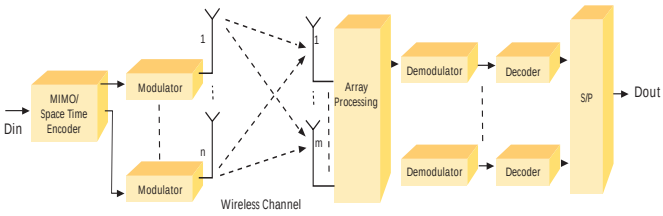


Figure 1 Block Diagram of MIMO System

OFDM technology coupled with efficient channel coding techniques and MIMO schemes and adaptive modulation techniques enable us to build efficient next generation broadband wireless communication systems. In the following sections, the OFDM and MIMO technology aspects are briefly discussed followed by the description of an OFDM based end-to-end baseband transceiver with multipath channel model and Space-Time codec for a 2x2 MIMO System. The System incorporates:

- Adaptive data rates up to 25 Mbps per user
- Adaptive modulation (QPSK, 8-PSK, 16 and 64 QAM)
- Adaptive 256/*512/1024/2048/4096-point FFT length*
- Two levels of coding (RS and *Space-time trellis coded modulation*)

The simulations were carried out in SPW platform against all the technical issues described in 2.3 below.

2. OFDM Technology

The Orthogonal Frequency Division Multiplexing (OFDM) is a form of Multi-Carrier Modulation (MCM), which is the principle of transmitting data by dividing the stream into several parallel bit streams such that each of the sub-streams have a much smaller data rate. These sub-streams are then modulated on individual sub-carriers from a set of several carrier frequencies.

The advances in Digital Signal Processing (DSP) and Very Large Scale Integration (VLSI) technologies have made it possible to bring this technology to the doorstep of consumers at affordable costs. The concept of OFDM is to transmit the data in parallel modulated sub-carriers using frequency division multiplexing. The sub-carrier spacing is selected such that each sub-carrier is located at zeros of all the other sub-carriers in the spectral domain (figure 2). The modulation scheme of the OFDM sub-carriers can be selected based on the requirement of power or spectrum efficiency.

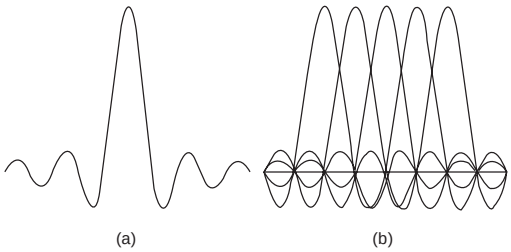


Figure 2 (a) An Unfiltered QPSK signal spectrum
(b) OFDM Signal spectrum

A "Guard Interval" separates successive OFDM symbols or OFDM frames in time domain. This arrangement shown in figure 3 is used to overcome the time dispersion of the communication channel (delay spread or ISI-Inter Symbol Interference). By using appropriate guard interval "T_g", the OFDM system can be made to operate in any hostile terrain with large delay spreads.

Figure 3 OFDM Frame Structure

The guard band is filled with cyclic prefix data because some signals must be transmitted instead of a long silence in order to maintain the receiver carrier synchronization. Also cyclic prefix data helps in modeling the transmission signal since cyclic convolution can still be applied between the OFDM signal and the channel response. However the guard band reduces data throughput. While ISI defines the minimum guard duration, increasing the useful symbol duration is limited by implementation issues such as carrier stability, doppler shift, FFT size and latency.

2.1 OFDM Modem Implementation

It can be mathematically shown that the OFDM spectrum is the real part of an Inverse Discrete Fourier Transform (IDFT) of the original data and generally IDFT is used in OFDM modulator. The mathematical analysis of OFDM is detailed in the following.

An N-point Inverse Discrete Fourier Transform is defined as:

$$x_p(n) = \sum_{n=0}^{N-1} x_p[k]\, e^{-j(2\pi/N)kn} \qquad (1)$$

Let $(d_0, d_1, d_2, \ldots, d_{N-1})$ be a data sequence, where each d_n is a complex number of the form a_n+b_n. For QPSK a_n, b_n = – 1 and for 16 QAM it is –1, –3. The data vector is represented as:

$$D_m = \sum_{n=0}^{N-1} d_n e^{-j(2\pi mn/N)} = \sum_{n=0}^{N-1} d_n e^{-j2\pi f_n t_m} \qquad (2)$$

where f_n =n/(NDT), t_k =kDt and Dt is an arbitrarily chosen symbol duration of the serial data sequence d_n.

The real part of the data vector Y_m is given by,

$$Y_m = Re(D_m) = \sum_{n=0}^{N-1}\left[a_n \cos(2\pi f_n t_m) + b_n \sin(2\pi f_n t_m)\right],\ k = 0,1,\ldots N-1 \qquad (3)$$

If these components are applied to a low pass filter at time intervals Dt, a frequency division multiplexed signal is obtained,

$$y(t) = \sum_{n=0}^{N-1}\left[a_n \cos(2\pi f_n t_m) + b_n \sin(2\pi f_n t_m)\right],\ 0 \le t \le N\Delta t \qquad (4)$$

The Fast Fourier Transform (FFT) is a faster computational tool for implementing DFT. The availability of this technique, and the technology that allows it to be implemented on integrated circuits at a reasonable price, has enabled OFDM implementations. At the transmitter, the signal is defined in the frequency domain. It is a sampled digital signal, and it is defined such that the discrete Fourier spectrum exists only at discrete frequencies. Each OFDM carrier corresponds to one element of this discrete Fourier spectrum. The amplitudes and phases of the carriers depend on the data to be transmitted. The data transitions are synchronized at the carriers, and can be processed together, symbol by symbol.

To summarize, the incoming serial data is first converted form serial to parallel and grouped into *x* bits each to form a complex number. The number *x* determines the signal constellation of the corresponding subcarrier, such as 16 QAM or 64QAM. The complex numbers are modulated in the baseband by the Inverse FFT (IFFT) and converted back to serial data for transmission. A guard interval is inserted between symbols to avoid intersymbol interference (ISI) caused by multipath distortion. The discrete symbols are converted to analog and low-pass filtered for RF up conversion. The receiver performs the inverse process of the transmitter. An equalizer compensates for the channel distortion and FFT process converts the signal to frequency domain where sub-carrier demodulation, decoding is performed.

2.2 OFDM Error Coding and Interleaving

The distribution of data over many carriers implies that selective fading will cause error in some of the received bits. By using error correction mechanisms, it is possible to correct many or all of the

errors in received bits. Usually convolutional coding is used with a viterbi receiver. As there is always a chance of residual errors after a viterbi decoder, some of the higher priority data could be pre-coded with a block code for additional security.

Interleaving the data before modulation can further improve the system performance. The data is interleaved both in frequency and time. The error correction works best if the errors in the incoming data are random. So the effects of burst errors must be minimized. To ensure this happens, the transmitted data is interleaved over all the carriers and over a range of time.

2.3 Technical Issues in OFDM

Any OFDM modem has the following technical issues that ought to be taken care of during design and simulations:

- Proper design of guard interval, interleaving and channel coding to compensate *ISI due to multipath propagation*
- The *peak-to-average power ratio (PAPR)* for a multi-carrier system is higher than that of single carrier system. The FDM signal could get clipped because of limited quantization levels, rounding and truncation during the FFT computation and other distribution parameters after D/A conversion during implementation. Proper design to take care of PAPR or a PAPR reduction scheme has to be implemented
- *Non-linear Distortion* due to non-linear devices in the OFDM signal path particularly the Power Amplifier in the transmitter has to be taken care of
- OFDM systems are very *sensitive to carrier frequency errors* caused due to phase noise and jitter in the local oscillators. Use of pilots or alternate schemes to track and correct for this is required
- *Carrier Recovery (Synchronization)/Equalization* mechanism to handle the frequency dispersion and doppler effects along with achieving time synchronization

3 Towards MIMO based systems

In order to increase the spectral efficiency (in other words to increase the channel capacity using the same bandwidth), a simple method is to increase the constellation points in the sub-carrier modulation. But this increases the required Noise immunity or the Signal-to-Noise ratio to achieve the same BER at the receiver putting an upper limit on the constellation size that can be used.

Systems with adaptive modulation can improve the data throughput by dynamically controlling the bit rate in both time and frequency domains in case of OFDM. It is assumed in this case that the transmitter knows the fading aspect of the wireless channel through say a feedback from the receiver. Adaptive modulation can hence improve the effective channel capacity.

Antenna diversity schemes could be used to improve the spectral efficiency. For instance one can use two (or more) antennas on the Transmit (Tx) side so that Tx diversity advantage can be imparted from Base Station to the Mobile terminal in the downlink. The Tx Diversity schemes could have a *feedback* mechanism in which the mobile sends a low data rate feedback to the Base Station like in 3G systems. On the other hand, the Tx diversity can also have *feed-forward* schemes like:

- Delay Tx Diversity – send time-delayed copy of the same data stream through the second antenna
- Permutation Tx Diversity – send a permuted (linear transformed) copy of the original symbol stream through the second antenna
- Space-Time Coded Tx Diversity – map the coded symbols to spatial channels to jointly accrue diversity and coding gains. The receiver in this case is the most complex compared to the other two but has the highest spectral efficiency.

Having multiple antennas on receiver side and array signal processing was described earlier. The recent developments to achieve higher channel capacities are to use MIMO systems, where in both the Tx and Rx sides have multiple antennas. As noted earlier, Space-Time Coding schemes enhance the performance of MIMO systems by providing coding gain in addition to spatial and temporal diversity gains.

The different types of ST codes are

- Layered ST Codes – simple one-dimensional coded bits are mapped to the Tx
- ST Block Codes – provide high diversity gain but nil to moderate coding gain.
- ST Trellis Codes – provide high diversity gain and high coding gain although the receiver required is complex (Viterbi decoder for ML decoding). In broadband design discussed below, ST Trellis coding have been used.

4 Broadband Wireless Communication System using OFDM and MIMO

Transmitter

The transmit chain contains the Scrambler, Reed Solomon Encoder, Space-Frequency Trellis Coded Modulator, Constellation Mapper, Time-Frequency Mapper, Pilot Insertion modules, IFFT, Cyclic Prefix Insertion modules, Pulse Shaping Window Function as shown in Figure 4.

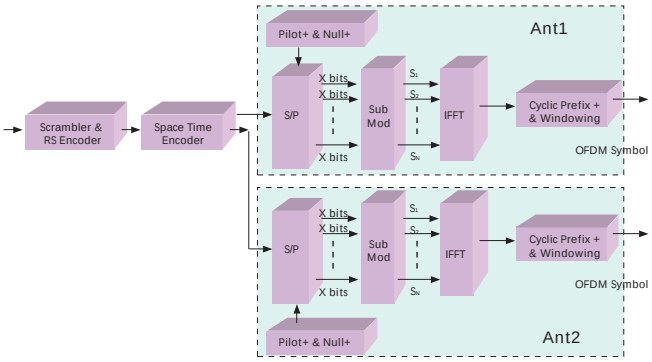


Figure 4 The 2-Antenna MIMO OFDM Transmitter

The input data is randomized to ensure uniform spectral energy and passed to the Reed Solomon Encoder, which provides the first outer

layer of forward error correction in our concatenated coding scheme. The Trellis Space-time Encoder provides forward error control for data transmitted over a MIMO channel. The Trellis Space-time encoder used is a rate _, tail-biting convolution encoder. Thus the coding rate of the encoder is always *1* and requires no bandwidth expansion. The ST encoder feeds out two symbol streams for the two antenna paths. Each output is fed to a serial-to-parallel Converter. The S/P breaks the input in groups of X-bits for modulating on to data sub-carriers. The pilot symbols and also the null carriers corresponding to pilot carriers are inserted. The value of X corresponds to the symbol length for the sub-carrier modulation and the number of S/P outputs corresponds to the number of OFDM sub-carriers. The Sub-carrier Modulator maps the X-bits in to relevant constellation points. The IFFT converts the frequency domain OFDM frame to time domain and then subjects it to cyclic prefix insertion and windowing.

Receiver

The signals from the two antennas are passed through a MIMO channel. The MIMO channel model includes fast fading due to doppler spreads and frequency selective fading due to delay spreads. The signal is received at the two receive antennas.

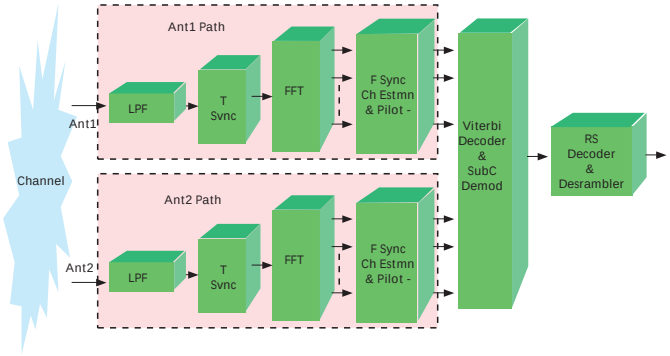
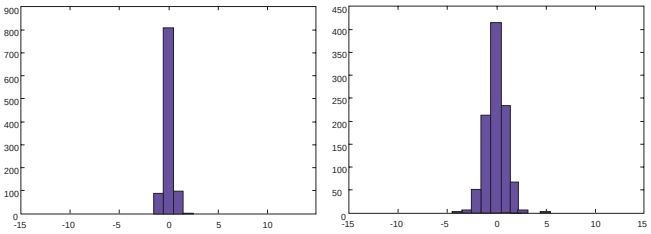


Figure 5 The 2-Antenna MIMO OFDM Receiver

The signals received at the two receiver antennas are independently processed until the viterbi decoder. The signals are low pass filtered (LPF) to remove the out of band noise. The timing synchronization followed by cyclic prefix removal is carried out and the time domain signal is subjected to FFT to convert to frequency domain OFDM symbols. The frequency and channel estimation are carried out using the pilot symbols, the channel is equalized thereby and fed to the Viterbi Decoder. The Vector Viterbi decoder performs Maximum Likelihood Sequence Detection decoding on the soft-decision symbols from the output of the Time-frequency demapper on the two received signal paths as shown in figure 5. The demodulated bits go through RS decoding and descrambling to recover the transmitted data ultimately.

The timing and frequency synchronization scheme based on pilot symbols were simulated. The probability distribution function (pdf) of frequency synchronization under different signal-to-noise ratios are shown in Figure 6. The BER performance for 256-point FFT and 8PSK with 2x2 MIMO compared to SISO is shown in Figure 7. The system simulation for all the cases including the analog artifacts could be carried out using SPW and its Matlab and C interface features. The GUI offered by SPW particularly the Interactive Simulation library helped to visualize all the simulation aspects very well.



SNR=20 dB SNR=10 dB

Figure 6 Pdf of Frequency Tracking Errors

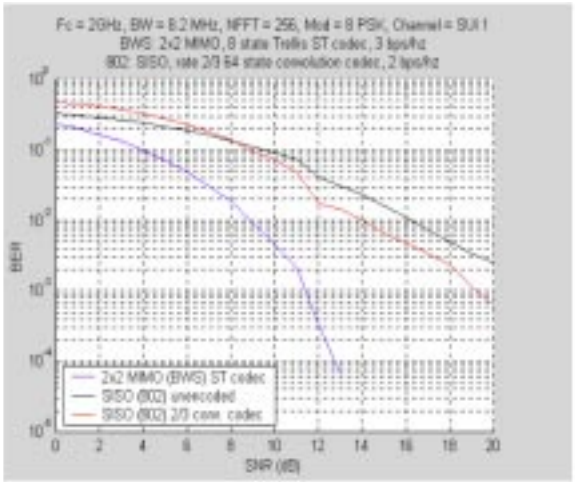


Figure 7 2x2 MIMO BER performance

[1] Orthogonal Frequency Division Multiplexing: A Multi-Carrier Modulation Scheme, Yiyan Wu, William Y Zou, IEEE Trans on consumer electronics, Vol.41, No.3, Aug1995.

[2] An Experimental Prototype Based on Wavefield Modeling for Wireless Broadband Non Line of Sight Communications at 155 Mbit/sec in 4 MHz, Max Martone, WJ Communications Inc.

Biography of Imtiaz:

Imtiyaz Mohamed worked in the Raman Research Institute, India from 1991 to 1996 where he was involved in designing millimeter and microwave receivers and other RF and digital systems for Radio Astronomy. He joined Maxtor Peripherals, Singapore and later moved to Centre For Wireless Communications now called Institute of Communications Research (ICR) in Singapore in 1997.

He worked in OFDM based Wireless ATM Research Project and was the R & D Manager for Wideband CDMA Terminal Development, joint projects with Ericsson and ST Microelectronics respectively in CWC. He joined Sasken Communication Technologies Limited, India in 2001 and has been working on OFDM based broadband systems and manages diffuse optical research programme. He has also worked on different wireless systems like PHS, Ultra Wideband (UWB), IEEE802.11a based WLAN Systems and has interest in the next generation wireless technologies. He holds a Bachelor of Engineering degree in Electronics from Bangalore Institute of Technology, India and Masters in Electrical Engineering from National University of Singapore.