Department of Electrical and Computer Engineering
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Technical Proposal:

Title: A 0.25um, Low-Jitter Multi-Phase PLL for Oversampling Data Recovery

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Abstract

This document outlines a proposal for the design of a 12-phase, monolithic phase-locked loop (PLL) for implementation in flat panel displays. Historically, PC's have always transmitted data to standard CRT's using analog transmission. However, as the popularity of flat-panel displays (FPD) has increased, analog transmission of data has become more redundant. The reason being that flat panel displays use digital graphics controllers to implement the image on screen, so the transmitted analog signal has to be converted back to digital format before it can be processed by the FPD.

Unfortunately, a critical bottleneck exists in the digital transmission between flat panel displays and personal computers. The problem is that cable connector imperfections and noise interference can result in intolerable bit-error rates for display imaging. Subsequently, a digital phase-locked loop method of data recovery has been proposed in [1] that can overcome these problems. Consequently, this method of digital data transmission has gained such popular acceptance that it has become the industry standard for flat panel displays. The PLL proposed here is ideally suited for implementation in such a digital phase-locked loop as described in [1].

The proposed 12 phase PLL implements a fully-differential design to reduce the sensitivity of the PLL on supply and substrate noise. The voltage-controlled oscillator (VCO) in the PLL consists of a current-starved, differential oscillator ring that is controlled by a differential loop-filter. An operational transconductance amplifier (OTA) will be implemented to convert the differential control loop voltage into a control current for the current-starved oscillator ring. The PLL also boasts a programmable charge pump and common-mode feedback circuit for the loop filter, to ensure the widest range of operating frequencies is achieved. Consequently, the PLL topology described in this proposal is a new and novel architecture and one that offers practical significance to the flat panel display industry.

1 INTRODUCTION

1.1 Purpose

The purpose of the project is to design and simulate a novel fully dfferential Phase-Locked Loop using quarter-micron technology.

1.2 Background

Phase-Locked Loops (PLLs) are standard components on almost all modern Integrated Circuits (IC). Their uses range from frequency synthesis (ie. to increase or decrease the period of a given periodic signal), to data recovery, to minimizing clock skew on large ICs.

The frequency synthesis PLL is of utmost importance in band-limited communication systems because it provides a means of generating a signal frequency many times higher than the one that is input. This is extremely important in transceiver systems that support only a limited bandwidth in certain areas. Thus, a low-frequency signal may be transmitted through a band-limited channel and converted to the necessary higher frequency signal by the PLL.

Because of the extreme importance of PLLs in today's architectures, a great deal of research and literature on the topic emanates from some of the top minds in the IC industry and the academic field. The current state of knowledge of general PLL mathematical interpretation, design and fabrication is vast; however, research does not exist for the design of a PLL in the specific implementation we are proposing.

PLL's are very challenging because internal circuits must be both digital and analog. In fact, although both the inputs and outputs of the PLL are digital signals, all internal circuitry is essentially analog. It is the analog areas of the PLL that require the most design experience and are the most difficult to test.

1.3 Rationale

The area of application for our PLL is high-speed digital data recovery. Flat Panel Display (FPD) ICs require a high-frequency, low-jitter PLL to receive and decode their input data signals. The PLL we propose is perfectly suited for this specific application. Thus, our main rationale for proposing this PLL is the Flat Panel Display market and its potential growth as an industry.

1.3.1 Flat Panel Displays

Flat Panel Displays (FPDs) are poised to overtake the display technology market over the next five years. The most popular of current FPDs are active matrix or Thin Film Transistor (TFT) flat panels. Using liquid crystal technology, FPDs are the most viable alternative to the current bulky computer monitors (Cathode Ray Tube or CRT displays). These new displays offer the advantages of lower desktop area, less eye-strain with almost no radiation, and much less power consumption compared with CRTs.

The FPD industry is already a multibillion dollar success in spite of the fact that FPDs cost 100-200% more than CRTs. Even at this premium, high-end consumers and large companies are willing to pay for the advantages offered by FPDs. Average consumers surveyed say that they would be indifferent about purchasing an FPD versus a CRT once the FPD price is 30% greater than CRTs [2]. Stanford Resources predicts that the cost of producing FPDs will hover around this important level by 2005, when CRTs will be all but extinct.

Although FPDs comprised of only 2% of all monitors shipped in 1998, market share is growing exponentially. By 2005, it is expected that FPDs will dominate the multi-use monitor industry. At that point, the FPD industry will reach revenues of close to $15 billion (US) [2].

1.3.2 Why Digital Interfaces?

The recent (April, 99) Digital Video Interface (DVI) Specification [3] released with the approval of most of the industry's major players (Intel, Silicon Image, Genesis) portrays the direction that FPD interfaces are taking in the near future. Currently, 90% of personal computers output an analog (RGB) signal to its respective CRT monitor. Thus, most current FPDs contain high-speed Analog to Digital Converters (ADC) to regenerate digital signals required by the FPD.

This means that currently, video signals generated by computer graphics accelerators are initially digital, converted to an analog signal for transmission to the FPD and then converted *back* to a digital signal inside the FPD. This redundant and inefficient interface will be phased out by the much more effective DVI digital interface over the next three years. Thus, the use of a purely digital interface increases the bandwidth of the PC-to-FPD interface as well as eliminating the need for the costly digital-to-analog converter (DAC) in the transmitter and the ADC in the receiver.

1.3.3 Additional Rationale

This project was also undertaken to enhance the knowledge base for PLLs used in certain receiver applications. Since the DVI Specification was only released in April of this year, knowledge and published research of PLLs used in this application is extremely scarce at this point. Although a few papers exist that define the DVI Interface and its exact requirements, no published research yet exists for the physical implementation of this system. We plan to make ground-breaking research in this novel area of relative obscurity.

Finally, we chose this project because of inherent level of difficulty. A PLL is fundamental device in an analog designers' knowledge handbook. Being undergraduate students with only a tip-of-the-iceberg understanding of complicated analog circuits, we believe this project will greatly enhance our knowledge of analog design. We also believe that the intellectual property extracted from this project may prove a worthy asset in the future.

2 Literature Survey

In this section of the proposal, five journal articles will be reviewed and their relevance as background material to this project will be outlined. Although many relevant articles were found during the background research of the multi-phase PLL, these five articles contributed the most significant amount of intellectual property. The focus of the articles range a wide array of topics, such as PLL design, jitter analysis in ring oscillators and a proposal for an over-sampling data-recovery circuit that can be used for flat-panel displays.

2.1 1.04 GBd Low EMI Digital Video Interface System Using Small Swing Serial Link Technique [1]

This paper provided the motivation for a high-speed, low-swing serial receiver and outlined how this design could overcome channel-to-channel skew problems encountered with digital NRZ transmission over twisted cable pairs. It also outlined how such problems currently existed for flat panel displays and that such a data-recovery circuit was essential for the future growth of the flat panel industry.

The digital phase-locked loop topology fundamentally consisted of three components. The first major section was a receiver that converted the differential signal to a single-ended digital signal and provided the correct termination resistance for the current-mode transmission. The next component was a phase-picking section that over-sampled the received data and used digital logic to determine the correct sequence of data. Finally, the last component was a charge pump PLL that generated 12 evenly phase-spaced clock signals to be used for the data over-sampling. However, in this article there was not a description nor a reference as to how this multi-phase PLL was designed. Consequently, this provided the motivation for the design of a multi-phase PLL that could be implemented into such a circuit [1].

This was not the first article published that described how a digital phase-locked loop could be used with over-sampling to recover serialised data [4-6]. However, it was the first to propose a circuit that was specifically designed for flat panel displays. The reason was that the proposed circuit required just 12 clock phases rather than 24 or 32 as described in [5] and [6], and as a result, it could be used to recover serialised data transmitted at frequencies in excess of 1GHz. This was essential if XGA resolutions were to be implemented on flat panel displays. As a result, the multi-phase PLL designs in [4-6] were not suitable for the data-recovery circuit used in [1]. The multi-phase PLL's described in [4-6] were older designs, and were developed for larger technologies. They also did not suppress the phase-to-phase jitter sufficiently to allow this proposed data-recovery method to work reliably.

2.2 A PLL Clock Generator with 5 to 110 MHz of Lock Range for Microprocessors[7]

This article described a microprocessor clock generator that was implemented using an analog phase-lock loop. The PLL was fabricated onto a 1.2 million transistor microprocessor in 0.8um CMOS technology without the need for any external components (i.e. precision loop filter resistors or capacitors). The PLL operated over a frequency range of 5Mhz to 110 MHz. The clock skew between the generated clock signal and the reference clock signal was 0.1ns. The PLL also had a peak-to-peak jitter of less than 0.3ns for a 50 MHz clock frequency.

The article provided preliminary circuit schematics for the entire PLL (i.e. PFD, charge-pump, LPF, VCO). It justified the implementation and described the key design parameters of each circuit. The PLL described in the article used a differential delay element in the VCO that was the same as the one described in this proposal. It was based on a P-MOSFET source coupled pair with voltage-controlled resistor load elements. The article also described why when choosing a VCO circuit, it was important to consider the control voltage versus frequency characteristic, because a linear characteristic would minimise the VCO sensitivity as a function of control voltage or operation frequency. As a result, this would provide the PLL with stability over the widest possible of frequency range.

The VCO in the article used a replica biasing circuit, similar to the one proposed for this project, to vary the load resistance in each delay element. It described that by varying the resistance such that the output swing remained constant, the VCO frequency would be linearly dependant on the control voltage as desired.

This article has become quite renowned concerning the design of PLLs and was referenced frequently in other articles because the author proposed the use of robust, differential analog circuits, that provided high power supply noise rejection, and ultimately reduced peak-to-peak clock jitter.

However, one major difference between the VCO described in this article and the one implemented in the multi-phase PLL is that the control voltage in the article was a single-ended signal referenced to VSS. Since, the low-pass filter had a capacitor connected to VDD, fluctuations on VDD injected noise on the control voltage and ultimately on the timing of the clock signal. Secondly, the V-I converter used in this article was simple and was not designed to provide substantial power supply noise rejection. Overall though, the techniques and circuits outlined in this article were very useful and as a result, it was constantly referenced during the design of the multi-phase PLL topology.

2.3 Fully Integrated CMOS Phase-Locked Loop with 15 to 240 MHz Locking Range and ± 50 ps Jitter[8]

This article described the structure of a fully integrated phase-locked loop that was implemented in a digital 0.5um CMOS technology. The PLL was quoted as having a 15MHz to 240MHz locking range. The static phase error was less than ± 100ps, with a peak-to-peak jitter of ±50ps at a 100MHz output frequency. The PLL had a resistorless architecture that was achieved by the implementation of feedforward current injection into the current controlled oscillator.

A major discussion in this article focused on the current injection into the ICO to substitute for a resistor in the low-pass filter. The motivation behind this alteration in the contemporary PLL structure was to provide area savings in terms of a reduced low-pass filter size. However, this topology had some definite trade-offs such as increased design complexity, instability problems and several other key issues as described in the article [8]. However, the most useful aspects of this article to the multi-phase PLL, were the use of a differential control voltage and an OTA to generate the tail current for the ring oscillator. Both the charge pump and low pass filter were fully differential. The loop filter also had a common-mode feedback circuit that increased the output dynamic range by maintaining constant common-mode voltage at the loop-filter capacitor.

The differential control voltage of the PLL was subsequently converted into a current through the use of an operational transconductance amplifier (OTA). OTA's are popular, well documented circuits used in continuous time filters (or more commonly known to analog designers as Gm-C filters). The author chose to use an OTA that consisted of two differential amplifiers that were connected in such a way that the current from the second differential pair added to the current from the first pair but in opposite phase. This topology allowed the transconductor to have a linear V-to-I characteristic over a wider operating range, which resulted in the PLL having a wider frequency range.

This article proposed that a differential delay cell could not reduce the jitter introduced by noise on the single-ended control voltage. As a result, the author introduced an alternative low-pass filter and VCO structure that resulted in smaller measured jitter characteristics than other published PLL structures of that time [7]. The compelling advantages offered by the complete differential structure determined that the multi-phase PLL should also incorporate a differential loop filter, to further reduce the sensitivity of the PLL to power supply noise.

In retrospect, this article did not introduce any new or novel circuit designs or analysis. Rather, it introduced a novel way to utilise contemporary circuit blocks in a new arrangement to create a PLL architecture with improved noise immunity. As a result of this, this article contributed greatly to the background research for the multi-phase PLL.

2.4 A Low-Jitter PLL Clock Generator For Microprocessors With 340 to 612 MHz Lock Range[9]

This article introduced the design of a PLL clock generator for the IBM Power3 microprocessor. It was implemented in a 2.5V, 0.4um digital CMOS process. The PLL used a fully differential, delay-interpolating VCO that was tunable over a frequency range determined by programmable frequency limit settings that reportedly enhanced yield and application flexibility. The article claimed that the PLL operational frequency range varied from 340MHz to 612MHz. The charge-pump current for the PLL was also programmable for additional control of the PLL loop dynamics. A fully differential loop filter was implemented into this design, with common mode stabilisation, which improved the noise rejection. Cycle-cycle jitter measurements with the microprocessor active were 80ps peak-peak with all measurements taken from the clock tree. Cycle-cycle jitter measurements with the processor in a reset state were 62ps peak-peak. The power dissipation of the PLL was less than 100mW.

The introduction provided references to literature that demonstrated that power supply noise created by the digital switching activity on a microprocessor was the dominant source of PLL jitter. He used these references to show how the primary focus of designers has been directed towards reducing this sensitivity. He followed this by revealing the measured jitter values from his design and compared them to other jitter values that were quoted from articles of the time [7][10]. Prior to this article, the lowest reported peak-peak jitter for inactive processors was 82-83ps and a PLL on a small (600K transistor) graphics display chip was reported with 80ps peak-peak jitter for a quiet supply at 320MHz [11]. This comparison demonstrated the superior noise resilience of the author's fully differential PLL design.

However, one significant reason for the decreased supply noise sensitivity of this PLL was because of the type of oscillator ring chosen. The author implemented a delay-interpolating ring oscillator [12][9][13] in contrast to the current-starved VCO's, that are very commonly used for microprocessor clock generators. Delay-interpolating VCO's have relatively low to moderate VCO gains and are well suited for fully differential control and signal path circuit implementations. The lower VCO gain of the delay-interpolating VCO's produce significantly less jitter due to coupled noise than higher gain structures. However, the limited operating frequency range for delay-interpolating VCO's had to be augmented by implementing significantly larger divider ratios, and by adding programmability to the VCO signal paths.

Unfortunately, in order to generate 12 phases from a delay-interpolating VCO, at least 12 delay elements and 6 mixers would be necessary for the design of the multi-phase PLL. Subsequently, this would increase both the complexity and the power consumption of the VCO. As a result, this type of VCO was not chosen for the design in this proposal. However, the outstanding performance of the PLL in this article did motivate the use of a fully differential charge-pump and low-pass filter in the multi-phase PLL design. In fact, many of the circuits used in the article can be found in this proposal (See Section 4: Methods and Motivations).

2.5 A 3-V 1.3-to-1.8-GHz CMOS Voltage-Controlled Oscillator with 0.3-ps Jitter[14]

This article presented a 3V, three stage VCO implemented in a 0.5um CMOS technology. The VCO used an active-feedback bias circuitry and swing-limiting devices to enhance its operation. The proposed VCO achieved a very wide operating frequency, from 1.3 GHz to 1.8GHz, with a relatively constant output amplitude and excellent linearity between the output frequency and the input control current. Both theoretical and simulation results were provided and showed that the predicted RMS timing jitter was as small as 0.3ps. The quoted power supply sensitivity was 5.5%/V and the power consumption was 23mW, solely for the VCO.

This article provided more than just circuit implementations of a current starved ring-oscillator. It also provided very important and insightful analysis into the performance and noise sensitivities of differential, current-starved oscillators. The article first introduced and developed an analytical expression which related the oscillation frequency of an oscillator to design parameters, such as the output swing of the oscillator, the control current, the load resistance and transistor sizings. It also analytically showed that by maintaining the output swing of each delay element constant, regardless of the tail current, the oscillator should have a linear dependence between frequency and control current. Although, this has been mentioned in other references [7][15], it has never previously been demonstrated analytically.

The article developed many other relevant and practical analytical results. Another demonstrated why the DC gain of delay elements in oscillator rings should be greater than 2, but not very large. The authors proved this by using the frequency domain transfer function of a delay element to show that oscillation could not be achieved unless the DC gain was greater than 2. However, and more importantly, the authors went on to develop a restriction on the DC gain that demonstrated the proportional relationship between DC gain and thermal noise. Many other articles have described the effects of thermal, shot and flicker noise on ring oscillators [16][17], however none of them were able to describe both the effect of the noise on timing jitter and in terms of critical circuit design parameters. As a result, this article and [18] provided excellent tools with which to design the oscillator by.

An example of how these articles can aid in the design of an oscillator is that the frequency of the oscillator and the peak-peak jitter caused by thermal noise can be approximated analytically prior to any simulation. Secondly, these analytical tools allow critical design parameters to be determined early on in the design stage. As a result, the approximate sizings of transistors can be optimised using these expressions, which will significantly reduce the simulation time required to design and optimise the circuit. Also, complex relationships such as thermal noise are very difficult to simulate and model, so these expressions provide the designer insight into how key design parameters effect the performance of the circuit.

3 Objectives and Hypotheses (Design Specifications)

As discussed before, our proposed PLL has an intended use in digital data recovery circuits in FPDs. Thus, we have a well-defined design specification from industry-released data.

Our proposed PLL will be a current-starved, fully-differential, low-jitter design with multiphase outputs. Before the quantitative values of our design specifications are displayed in chart format, we will explain the reasons for implementing our PLL in its unique manner.

3.1 Fully-Differential Analog Blocks

For PLLs, a fully-differential implementation is rarely found. Although most PLLs have a fully differential Voltage Controlled Oscillator (VCO), it is not common to find a design with a fully differential Loop Filter to be implemented with a current-starved ring oscillator. We chose this more complicated implementation because it more readily rejects power supply noise, which is the main source of jitter in PLLs. Specifics on this topic will be discussed in the *Methods and Materials* in section 4.

3.2 Low-Jitter

The PLL required for the intended application must be a low-jitter design. For data recovery implementations, any jitter introduced greatly increases the probability of a bit error and thus increases the Bit Error Rate (BER). This is very important because the BER is the main criterion used in evaluating the quality of a data recovery circuit. A higher BER equates to a poorer data recovery circuit.

3.3 Current-Starved VCO

There are three main oscillator design methodologies: relaxation, current-starved and delay-interpolating oscillators. We chose the current-starved design due to the PLL's requirement to output 12 equal phases. The current-starved method requires only six inverting stages in the VCO. However, the delay-interpolating method would require twice as many inverting stages for the same result. Thus, the current starved methodology in the VCO is much simpler and takes less than half the power and area as compared with the delay-interpolating method. Furthermore, the relaxation oscillation method is incompatible with our requirements for multiphase outputs. Again, more details on this will be discussed in the following section.

3.4 Multiphase Outputs

The implementation for which our proposed PLL is being designed for requires 12 equal output phases each 30° apart. The best way to implement this is to use six differential inverting stages and to tap off both outputs at each stage. This methodology gives the required output of 12 equally spaced output phases with the least amount of hardware and area.

3.5 Specifications of the Proposed PLL

FEATURE	DESCRIPTION
Power Supply (Vdd)	2.5V, isolated analog and digital power supplies
Technology	0.25um
Gate Length	1.0um (to eliminate short channel effects)
Cycle-to-Cycle Jitter	Maximum 80 ps, 10ps RMS
VCO	• Six differential inverters with 12 tap offs for the outputs • Current starved design • Input is a differential control voltage from the Loop Filter. • An Operational Transconductance Amplifier (OTA) will be used to convert the differential input voltage to a current for mirroring • Gain of each stage is kept constant using a negative feedback implementation on the symmetrical, linearised load resistors • Because of the constant gain, the Voltage-Frequency relationship is linear over a wide range
Loop Filter	• Fully differential implemention for maximum power supply noise rejection • Differential V_{ctnl}^{+} and V_{cntl}^{-} as outputs fed into the VCO • Highly robust design
Phase Detector	• Fully digital design • Digital outputs $V_{pull\text{-}up}^{+}$, $V_{pull\text{-}up}^{-}$, $V_{pull\text{-}down}^{+}$, and $V_{pull\text{-}down}^{-}$ are fed to the Loop Filter
Divider Circuit	• Fully digital design • Divide by 2.5 circuit for our required implementation
Programmability	To vary the locking time and closed-loop frequency response of the PLL, 2 extra bits are added to the design to provide a programmable charge-pump current.
Testability	Each of the four components will have test structures for individual verification.

3.6 Reset

The reset signal will be used to initialize the PLL to a known state, and at the same time, force it to start the acquisition process. The PLL must be reset to ensure proper locking should one or more of the following situations apply:

1. at power up;
2. after waking up from Powerdown Mode;
3. reference and/or feedback clock sources changed;
4. reference clock frequently changed.

3.7 Powerdown Mode

The PLL can be put into Powerdown Mode by de-asserting the signal IPLLEN (active high). Switching activities at all input pins should be stopped in Powerdown Mode. The PLL consumes no current (except the tiny inevitable leakage current) when it is powered down. To “wake up” from Powerdown Mode, simply assert IPLLEN. In addition, the PLL must be reset (to start the acquisition process) before it can become functional (locking) again.

4 Methods and Materials

4.1 Overview of PLL Topology

The basic circuit topology for the charge-pump PLL is shown in Appendix 1, Figure 1. It incorporates a phase-detector, differential charge-pump and loop-filter, a fully differential VCO and a frequency divider. Typically in PLLs, supply and substrate noise are the major contributors to timing jitter. As a result, to reduce the jitter of the multi-phase PLL, a fully differential design will be implemented for all of the critical analog blocks of the PLL (i.e. charge pump, low-pass filter, voltage-to-current converter, VCO delay element). Separate power and ground pads will be used for the analog and the digital components of the PLL. The architecture of a fully differential, current-starved PLL was originally published by [8], however it was not a multi-phase PLL as proposed by this project. As a result, the proposed fully-differential design is a rather novel architecture to be used for a charge-pump PLL.

The next several sections describe the proposed architecture for each of the main building blocks of the multi-phase PLL as follows:

- Section 4.1.1: Voltage-Controlled Oscillator describes the architecture and motivation for the proposed design of the differential V-to-I converter, current-controlled oscillator and replica biasing circuits.
- Section 4.1.2: Differential Loop Filter, initialisation circuit and common-mode feedback circuit.
- Section 4.1.3: Differential Charge Pump
- Section 4.1.4: Phase Detector

4.1.1 Voltage-Controlled Oscillator

The most critical part of the PLL is the ring oscillator. It is the part of the PLL that generates the clock signals. However, it is also responsible for most of the timing jitter introduced on the clock signals. The multi-phase PLL will be implemented using a current-starved, differential ring oscillator. Typically there are three common circuit topologies for integrated VCOs: the relaxation, the delay-interpolating, and the current-starved VCO. The relaxation VCO operates by charging and discharging a timing capacitor with a constant current. Varying the current magnitude varies the frequency of the VCO. This type of VCO uses few transistors and small timing capacitors, it also has a wide tuning range and dissipates little power. However, since the voltage across the timing capacitor crossing a switching threshold determines the frequency of operation, it is very susceptible to timing jitter from substrate and supply noise [12]. Secondly, this type of oscillator can not be used to generate multi-phases; as a result this type of VCO was incompatible with the objectives of the design.

A second common type of VCO is a variable-stage or delay-interpolating VCO [19]. This type of VCO consists of two delay lines of different lengths. The output of the delay lines are combined in a multiplexor, or mixer. The multiplexor acts as an analog mixer and continuously tunes the effective delay as a combination of the two delay lines. This type of oscillator has been found to have excellent power-supply noise rejection [12][9][13] because of the fully differential design and the typically low-gain of the VCO. However, to implement a 12-phase VCO using this type of architecture requires a significant amount of circuit complexity and increased power dissipation. As a result, this type of VCO was also rejected for this design.

The third type of VCO is the current-controlled, or current-starved, ring oscillator [7][20][21]. The basic concept is to control the current in each stage of the ring oscillator in order to vary its delay, and hence the frequency of operation. This type of oscillator can achieve a wide range of frequencies and can easily be implemented to produce the 12 phases that the project requires. As a result, a current-starved ring oscillator was chosen to be implemented in the multi-phase PLL as shown in Appendix 1, Figure 2.

The ICO circuit will be designed to have minimum power supply and substrate noise sensitivity, and at the same time, provide a wide and linear range of frequency operation. The ICO will consist of six delay elements and each delay element will be fully differential and consist of a source-coupled PFET pair driving symmetrical load elements comprised of a diode connected NFET and a variable NFET current source (See Appendix 1, Figure 3). The current source will be implemented using cascoded current mirrors to increase the impedance of the current source and to increase power supply noise rejection. The input differential pair will be implemented using PFET input transistors to reduce substrate noise and body effect, because they can be implanted in an isolated n-well that is biased at the source voltage of the input PFET. By biasing the input pair in this manner, substrate noise will be significantly reduced in the input pair, thus reducing the overall timing jitter of the oscillator ring. The output voltage swing of each delay element will be maintained constant by using a replica biasing circuit and feedback to vary the resistance of the loads to compensate for changes in the tail current. This will increase the linear range of operation for the oscillator ring [15].

A transconductance stage (OTA) will be used to convert the differential loop-filter, control voltage inputs into current. This is the current that is subsequently mirrored by all of the delay elements and the replica biasing circuitry. The use of a differential OTA will also increase the power supply rejection ratio of the VCO.

4.1.2 Differential Loop Filter

The proposed differential loop filter and initialisation circuits are shown in Appendix 1, Figure 4. Current to and from the charge pump will enter the filter nodes CPPOS and CPNEG. The capacitors will be P-type, accumulation-mode gate-oxide devices. Their layouts will be interleaved to improve matching [15]. Either N-well or poly resistors will be implemented (depending on which is more precise for TSMC 0.25um process) to produce a zero in the filter transfer function. The filter output will be connected to the VCO at VPOS and VNEG. An initialisation circuit activated during the powering-on of the PLL will be used to pre-charge the filter capacitors to the nominal, common-mode voltages at nodes POSC and NEGC.

In a practical implementation, a common-mode voltage may appear on the filter due to leakage, drift or mismatch in the charge-pump and/or the filter. Since common-mode voltage can introduce frequency offsets and reduce the frequency range of the PLL, a common-mode circuit will be connected to the loop filter to ensure that a common-mode voltage is maintained. Secondly, the gates of the series connected NMOS transistors will be connected to AVDD (analog power supply), resulting in the maximum filter voltage to be AVDD-V_{tn} (where V_{tn} is the NMOS threshold voltage). Consequently, this will ensure that the VCO will not shut off because of a large loop filter voltage, although it should slightly reduce the operating range of the PLL.

4.1.3 Differential Charge Pump

A wide-swing, constant transconductance [15] circuit will be used to generate the currents I_O, $2xI_O$ and $4xI_O$ for use within the charge pump [9] (See Appendix 1, Figure 5). The value of the current used in the charge pump is programmable with three bits PC0, PC1, PC2. If a PC bit is high, it will connect the input of that cascode NFET to $V_{cascode\text{-}n}$, otherwise it will connect the input to ground. By making the charge pump current programmable, the performance of the PLL can be optimised for any various output frequencies. Programmability can also be a valuable testing tool, should the PLL be fabricated.

4.1.4 Phase Detector (PFD)

At this moment, it is still unsure what type of phase detector will be implemented. To minimize any jitter and phase error between the reference and output clock, the “dead zone,” of the PFD should be minimal. The “dead zone” occurs when the phase difference between the reference and feedback clock is minimal, such that the charge pump does not have time to turn on and correct the phase difference. The result of this is that a static, peak-peak jitter approximately equal to the width of the dead zone can arise at the output.

One possible implementation is a dynamic PFD, which has a significantly smaller delay on its critical path [22], and consequently suffers from a much reduced dead zone. However, one must always be careful of noise margins and crowbar currents when using pre-charged circuits, especially if a clock signal is absent for a long period of time. Another possible implementation is to have both the UP and DOWN signals come high for a sufficient amount of time before they are reset. This will ideally allow the charge pump to come on and correct the phase difference between the reference and the feedback clocks. However, since both the UP and DOWN currents will have some mismatch, the state where both currents are conducting will introduce some voltage error on the differential loop filter [23]. As a result, it is still undetermined which type of PFD will result in the least amount of dead zone and ultimately contribute the least amount of jitter.

4.2 Design Methodology

In order to accurately design the PLL such that it has satisfactory resilience against power supply, substrate and thermal noise, a proper design methodology must be implemented. Since analog circuits are much more difficult and sensitive to design than their digital counterparts, the following design methodology and verification will be used in the design of the PLL:

1. Research all relevant journal articles for the circuit, to determine which circuit architecture is most appropriate for this application.

2. Perform a preliminary analytical analysis of the circuit to understand exactly how it functions, what are the critical components of the circuit and determine critical design parameters such as: gain, frequency response (i.e. 3dB frequency), input/output resistance, signal-to-noise ratio, etc.

3. Use the analytical expressions, previously obtained, to approximately determine suitable transistor sizings such that the circuit meets the performance criteria of this application.

4. Use Hspice to simulate the circuit, verify and refine the critical design parameters (i.e. gain, frequency response (i.e. 3dB frequency), input/output resistance, signal-to-noise ratio, etc.) and determine the final transistor sizings such that the performance of the circuit is optimised.

5. After all of the PLL circuit blocks have been designed, except for the Low-Pass Filter, the entire functionality of the PLL will be modeled by a self-developed C program emulator. The emulator can model the performance of the PLL, using parameters that are entered into an input file (to see a template of the input file, see Appendix 2). By inputting the relevant values obtained from Hspice into the emulator, the performance of the PLL with different low-pass filters can be assessed.

   Another advantage of the emulator, is that it can simulate and model noise on the VCO (i.e. power-supply noise and substrate noise) to approximate what the typical timing jitter of the PLL would be under typical operating conditions. As a result, use of the emulator, will allow an optimised low-pass filter design to be determined.

6. Finally, if time permits, the entire PLL will be laid out using Cadence Virtuoso. Design rules will be checked using DIVA DRC and the connectivity will be confirmed using DIVA LVS. Finally, circuit parasitics will be extracted using DIVA LPE and the final, post-layout simulation of the PLL will be performed using Hspice. This will be the final, most accurate simulation of the PLL prior to fabrication.

4.3 Analytical Device Modeling

As described in Section 4.2, prior to simulation, all circuits will be described analytically to understand and model the critical design parameters of the circuit and to determine preliminary sizings for the circuit. If this is to be done with some sort of accuracy, the transistors must be modeled with analytical expressions that should somewhat match Hspice simulation results. As a result, this was completed prior to developing the proposal, as background to this project.

The common square-law relation for the current, gate-source voltage, and drain-source voltage was used to analytically model the performance of the transistors for gate lengths greater than 0.5um. Since shorter gate lengths than this suffer more drastically from short-channel effects, the analytical expressions less accurately predict the performance of these transistors. As a result, the analytical expressions derived will not accurately describe these short-channel transistors, so for design simplicity a standard transistor gate length of 1um will try to be used for all analog transistors. As, seen in Appendix 3, the analytical DC model for both the NFET's and PFET's closely match Hspice simulations for a 1um gate length, so it can be assured that preliminary analysis should accurately predict the performance of the circuit.

In reality, transistor current is not simply related to the inverse of the gate length as the square-law theory predicts. As a result, by trying to use one standard gate length for all of the analog devices, it should make both the performance and predictability of the analog circuits more reliable and easier to design. If higher currents and gains are required, a minimum gate length to be used will be around 0.5um. Below that, the transistors do not closely match the square-law current-voltage relations, as shown in Appendix 3. Since most circuits were designed using the square-law current-voltage relations, short-channel devices can result in unpredictable and unreliable circuit performance.

5 Timetable

The expected time to complete our project from the completion of this proposal is six months. We have divided our project into seven main phases. The seven phases are:

- Background research
- Approximating transistor models
- Designing the VCO
- Designing the Loop Filter
- Designing the Phase Detector
- Designing the Divider Circuit
- Amalgamating the blocks together

A concise description of each phase is below:

5.1 Background Research

Before any design of the PLL takes place, an exhaustive research phase to become familiar with the design requirements and previous PLL research will take place. This phase involves investigation of textbooks to become familiar with PLL fundamentals and analyzing various IEEE and industry released research papers for similar research.

5.2 Approximation of Transistor Models

The second phase of our project is to find estimate values for the parameters of the transistors we will be simulating. Using complex curve-fitting procedures, we will reduce complicated SPICE models into first-order approximations for use in our hand-design.

5.3 Design of the VCO, Loop Filter, Phase Detector and Divider Circuit

There exist four main blocks in the PLL and each will be completed individually. Since the analog blocks (VCO, Loop Filter) are the most challenging to realize, more time will be allotted for their design. Furthermore, the analog designs will be completing first chronologically to allow for additional time if required.

5.4 Amalgamation of the Blocks

The fifth phase of our design cycle is to combine the four blocks. This is essentially the polishing step used to smooth out any difficulties in block interfaces. We will also finalize all global testing and programmability issues across the PLL.

5.5 Gantt Timetable

Please see the attached timetable in Appendix 5 for exact completion dates and relevant sub-sections for each phase.

6 Resource Requirements

To design the complete PLL will require the following resources:

- HSPICE 97 license: to run our simulations
- AvanWaves license: to view our simulated waveforms
- Cadence license: for potential layouts, and DIVA verification
- Access to Matlab Software
- Access to 2 Unix workstations, one for each student
- Extra disk space (50-100 Mb) on ECF drives
- PC time for word processing and spreadsheet applications using MS OFFICE 97/2000

7 Budget

Since integrated circuits can only be implemented using Computer Aided Design (CAD) tools prior to fabrication, the cost of a monolithic design is rather inexpensive if the workstation and licenses have already been acquired. Subsequently, our proposed PLL will require the following expenses:

Expense	Cost
Computer Time (Hardware and Software)	$800 (at $50/month/student)
Materials and Supplies	$320 (at $20/month/student for photocopying, electronic supplies, telephone charges and stationary)

8 Expected Benefits

As outlined in this report, the proposed PLL is not just another phase-locked loop design to be added upon the heap of literature that currently exists on this topic. Rather, the proposed PLL architecture is new and novel and surpasses the scope of a typical undergraduate thesis. Beyond this, the proposed project offers practical significance to the Flat-Panel industry. As shown in section 1.3.1 Flat Panel Displays, the FPD industry is an exponentially growing market that is projected to overtake standard CRT yearly sales, shortly.

However, as outlined in the abstract, there is a current bottleneck that exists in the functional implementation of digital transmission between personal computers and FPDs. This has been overcome by a novel, digital phase-locked loop data recovery circuit as proposed in [1]. However, the design in the article required a 12 phase, analog PLL to oversample the transmitted data, but yet provided no implementation for this PLL. Subsequently, the PLL proposed here is ideally suited to be implemented in the data recovery block as described in [1].

Ultimately, the proposed PLL will add significantly to the small, but emerging literature concerning circuit implementations to be used in the design of Flat Panel Displays. It is a project with immediate relevance and has a possible financial benefit to a multi-million dollar, and ever-growing industry.

Appendix 1:

Methods and Materials Figures

Figure 1: PLL Topology

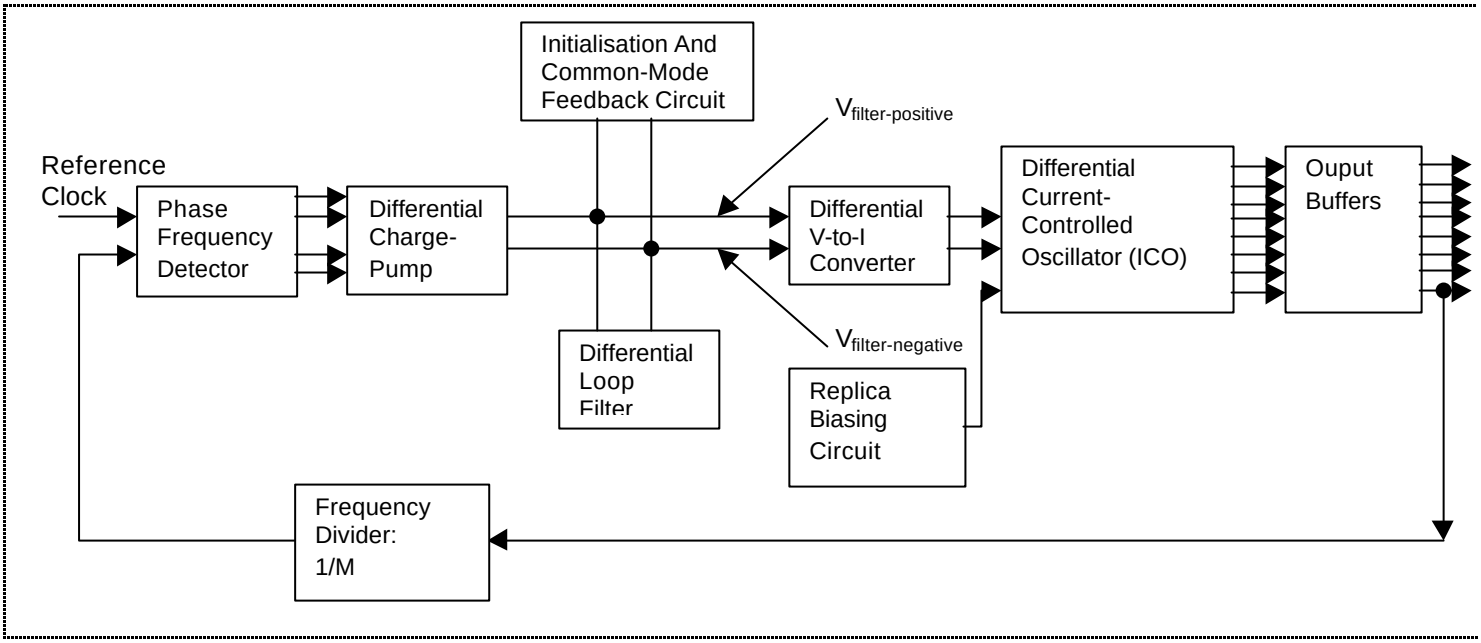


Figure 2: Architecture of Current-Starved Oscillator Ring

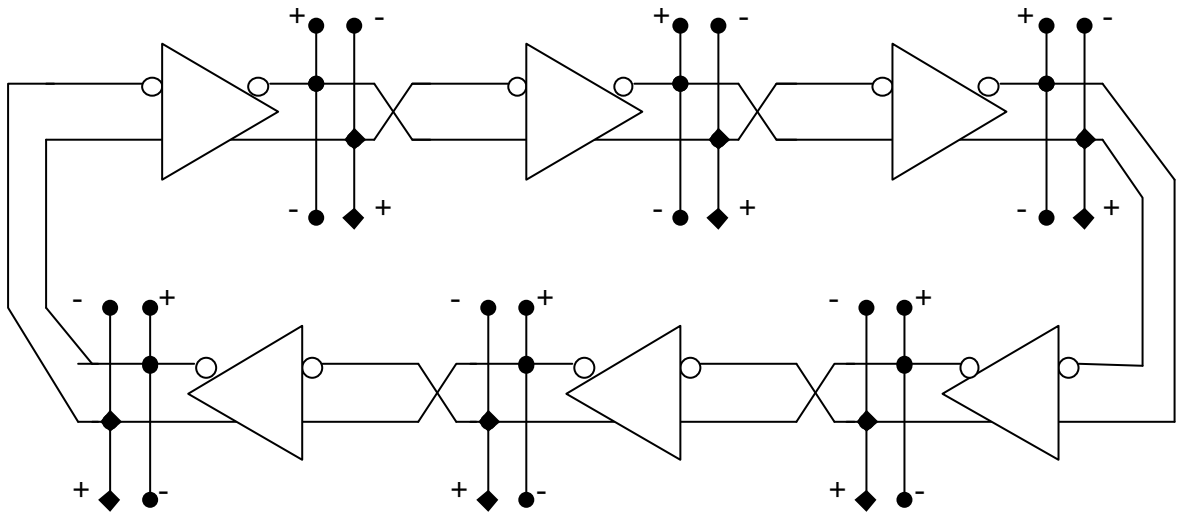


Figure 3: Proposed Schematics of a Delay Element and Replica Bias Circuit

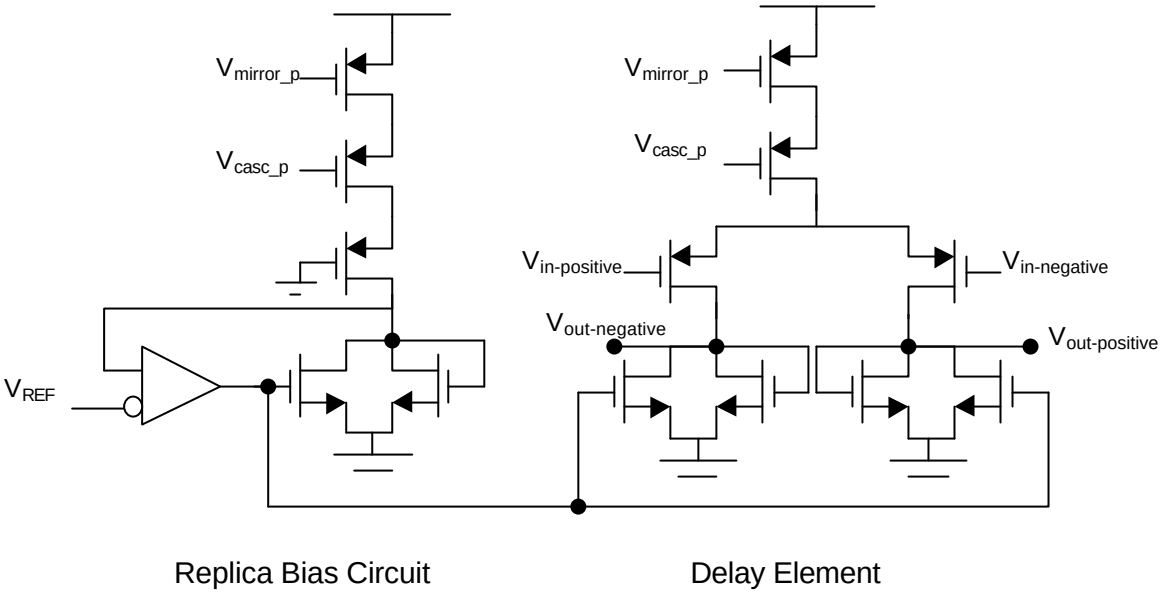


Figure 4: Proposed Schematics of the Differential Loop Filter

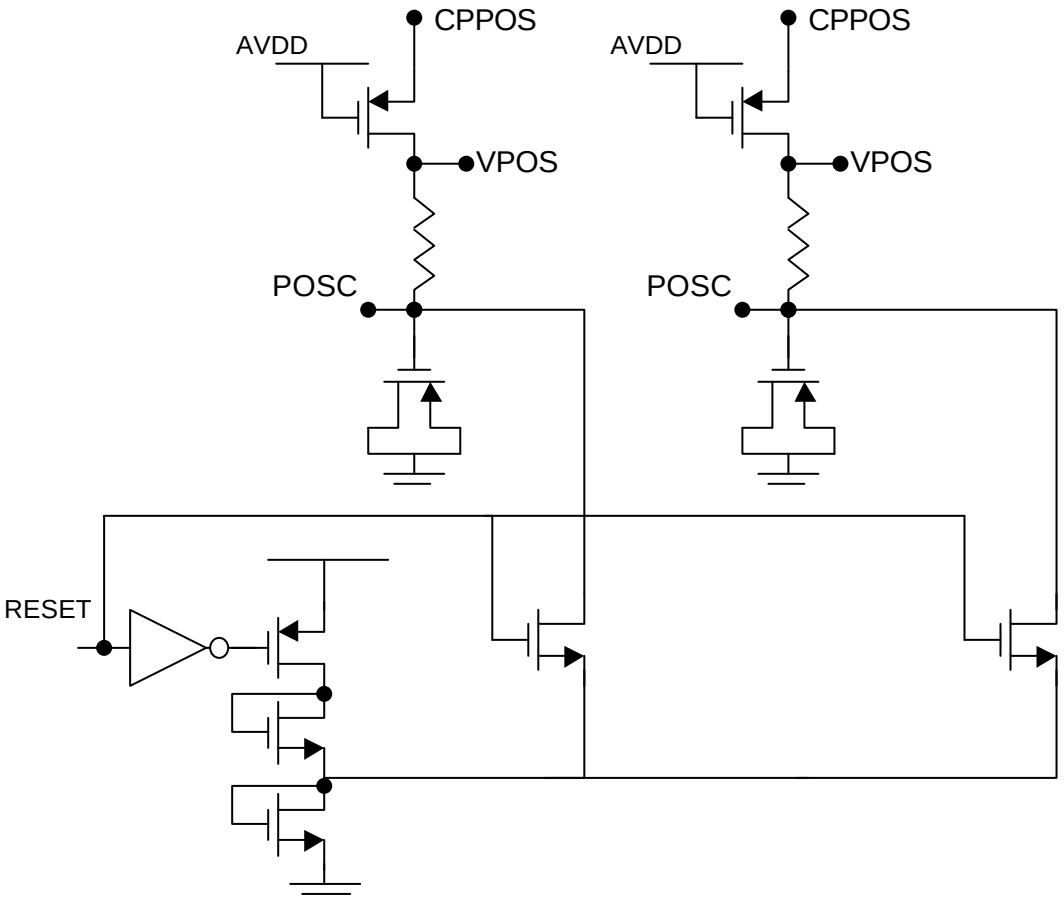
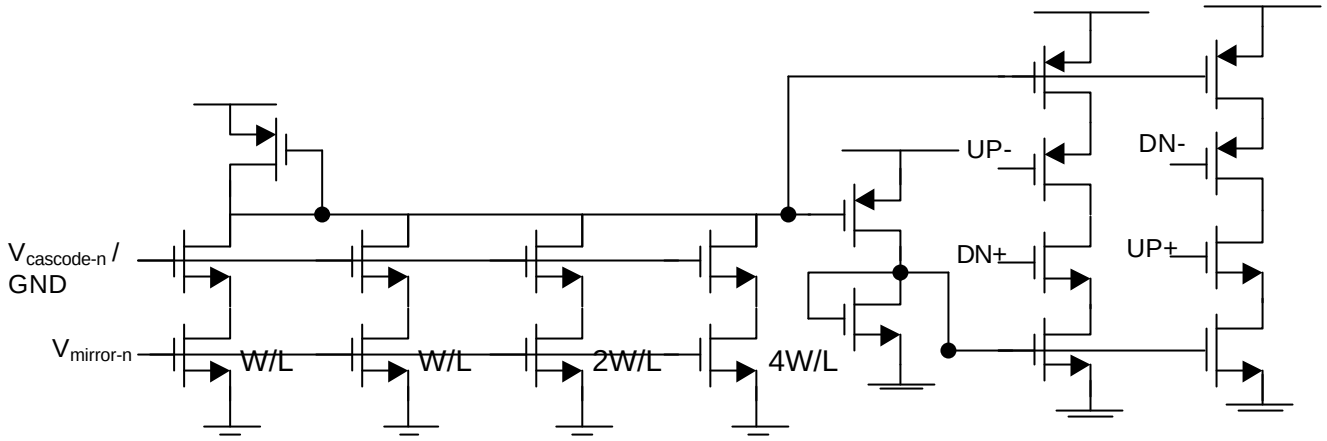


Figure 5: Proposed Schematics of the Differential Charge-Pump



Appendix 2:

Input Template File for Closed-Loop PLL

/ //
/ ////////////////////// This is a template for the input file ///////////////////
/ ////////////////////////////////PLL model //
/ //
/ //

/ Any line will be ignored when it is led with a "/"

/ You can also comment the end of a line by including a "/"

/ Any numerical data entered into the program may be represented by exponential
/ notation (ie.
/ 345.78e-9,-43.67e+09 etc.) or by a scale factor as follows:
/ f=1e-15
/ p=1e-12
/ n=1e-9
/ u=1e-6
/ m=1e-3
/ k=1e+3
/ M=1e+6
/ G=1e+9
/ Any of these scale factors must be used with the letter-case shown. Regardless of
/ whether scale factor notation or exponential notation is used, units may be appended to
/ data. If the incorrect unit is used an error will be output. Note: since resistence does not
/ have a single letter representation of its unit, when entered it should not have any units
/ appended to it. If it does, an error will be printed on the screen. Warning: you can only use
/ scaling factor notation or exponential notation exclusively !!! If not an error will be printed
/ !!! All noise types must begin with a letter and should not have units appended to them.
/ The error messages should be used to debug the input file.

/ //
/ //// The following data must be included for the simulation to succeed. ////
/ //

TRAN <<duration time of simulation>> <<printed time steps>>

VOUT <<initial voltage of VOUT at time t=0s (ex either VDD or VSS)>>
<<initial output frequency at time t=0s>>

PD <<time delay>> <<dual turn on time for both up and down>>
<<up jitter type>> <<down jitter type>>

CP <<time delay>> <<resistence in series with capacitor>>

<<optional :value of capacitor in series with resistor name of capacitor value data type>>
<<capacitor in parallel>> <<leakage resistence>> <<UP Current Source value>>
<<DOWN Current Source Value>> <<up noise type>>

VCO <<time delay>> <<noise type>>

M <<M value>> <<time delay>> <<noise type>>

VIN <<voltage at time=0s (ex.VDD)>> <<value of other voltage (ex.VSS)>>

/ Jitter on the reference clock can be modeled here.
VDATA<<number of datapoints entered>> /Edges of VIN
<<time of first edge>> <<time of second edge>> <<...>>
<<datapoints in seconds>>
ENDVDATA

/ ***VCO transfer function datapoints***

VCODATA <<number of sets of datapoints>>
<<voltage 1>> <<frequency 1>> <<VDD1>>
<<voltage 2>> <<frequency 2>> <<VDD1>>
<<...>>
<<voltage 1>> <<frequency 1>> <<VDD2>>
<<voltage 2>> <<frequency 2>> <<VDD2>>
<<...>>
<<voltage 1>> <<frequency 1>> <<VDD3>>
<<voltage 2>> <<frequency 2>> <<VDD3>>
<<...>>
ENDVCODATA

/ //
/ /// ***The following commands are optional for a simulation.*** ////////////////////
/ //

/ ***You can include up to 20 optional noise types. These noise types are defi*****ned**
/ ***by datapoints entered into input file.***
/ ***The template to enter the optional noise types is as follows:***

VDD_NOISE
<<first noise1 value>> <<second noise1 value>>
<<third noise1 value>> <<...>>

ENDVDD_NOISE

NOISE <<NOISE_NAME1>> <<number of datapoints>>
<<first noise1 value>> <<second noise1 value>>
<<third noise1 value>> <<...>>
ENDNOISE

NOISE <<NOISE_NAME2>> <<number of datapoints>>
<<first noise2 value>> <<second noise2 value>>
<<third noise2 value>> <<...>>
ENDNOISE

NOISE <<NOISE_NAME_n>> <<number of datapoints>>
<<first noise_n value>> <<second noise_n value>>
<<third noise_n value>> <<...>>
ENDNOISE

CAPSERIESDATA <<name of data type: must match the name entered in the CP line>>
<<number of data points>>
<<voltage 1>> <<capacitance 1>>
<<voltage 2>> <<capacitance 2>>
<<...>>
ENDCAPSERIESDATA

/ ***To be sure of the data that the program will use to simulate the PLL, include***
/ ***the following "PRINT" command in your input file. It will write out all of the / input file data*** / ***used in the simulation to a ".tx0" file with the same name as / your input file.***

PRINT /***Optional***

/ ***To write all of the data from the simulation out to a ".dat" file include the***
/ ***"PRINTDATA" keyword in your input file. It will write out all of the***
/ ***simulation data derived from the simulation to a ".dat" file with the same***
/ ***name as your input file.***

PRINTDATA /***Optional***

/ //
/ ///// ***END must be included in input file to indicate end of file.*** ////////////////
/ //

END

Appendix 3:

Results of Analytical Modeling of NFET's and PFET's for All Three Process Corners: Slow, Nominal and Fast

Table 1 shows the derived analytical values that model the behavior of the NFET under:

- nominal conditions (i.e. VDD=2.5V, temperature=25°C and nominal process corner)
- slow conditions (i.e. VDD=2.25V, temperature=100°C and slow process corner)
- fast conditions (i.e. VDD=2.75V, temperature=0°C and fast process corner).

Table 1

Transistor Type	Case	Operation Range	Region	$(1/2)U_NC_{OX}$	V_T	l
NMOS	SLOW	Vgs<0.65V	***Cut-Off*** Id=0	N/A	N/A	N/A
		Vgs>0.65V Vds<Vgs-0.3318	***Triode*** Id=(1/2)*Un*Cox[2(Vgs-Vt)*Vds-Vds^2]	$3.623x10^{-5}$	0.3318	N/A
		Vgs>0.65V Vds>Vgs-0.3318	***Active*** Id=(1/2)Un*Cox*$(Vgs-Vt)^2$ *(1+λ*[Vds-Veff])	$3.623x10^{-5}$	0.3318	$4.03x10^{-2}$
	NOML	Vgs<0.65V	***Cut-Off*** Id=0	N/A	N/A	N/A
		Vgs>0.65V Vds<Vgs-0.3318	***Triode*** Id=(1/2)*Un*Cox[2(Vgs-Vt)*Vds-Vds^2]	$5.89x10^{-5}$	0.3510	N/A
		Vgs>0.65V Vds>Vgs-0.3318	***Active*** Id=(1/2)Un*Cox*$(Vgs-Vt)^2$ *(1+λ*[Vds-Veff])	$5.89x10^{-5}$	0.3510	$4.47x10^{-2}$
	FAST	Vgs<0.65V	***Cut-Off*** Id=0	N/A	N/A	N/A
		Vgs>0.65V Vds<Vgs-0.3318	***Triode*** Id=(1/2)*Un*Cox[2(Vgs-Vt)*Vds-Vds^2]	$6.976x10^{-5}$	0.292	N/A
		Vgs>0.65V Vds>Vgs-0.3318	***Active*** Id=(1/2)Un*Cox*$(Vgs-Vt)^2$ *(1+λ*[Vds-Veff])	$6.976x10^{-5}$	0.292	$3.85x10^{-2}$

Table 2 shows the derived analytical values that model the behavior of the PFET under:

- nominal conditions (i.e. VDD=2.5V, temperature=25°C and nominal process corner)
- slow conditions (i.e. VDD=2.25V, temperature=100°C and slow process corner)
- fast conditions (i.e. VDD=2.75V, temperature=0°C and fast process corner).

Table 2

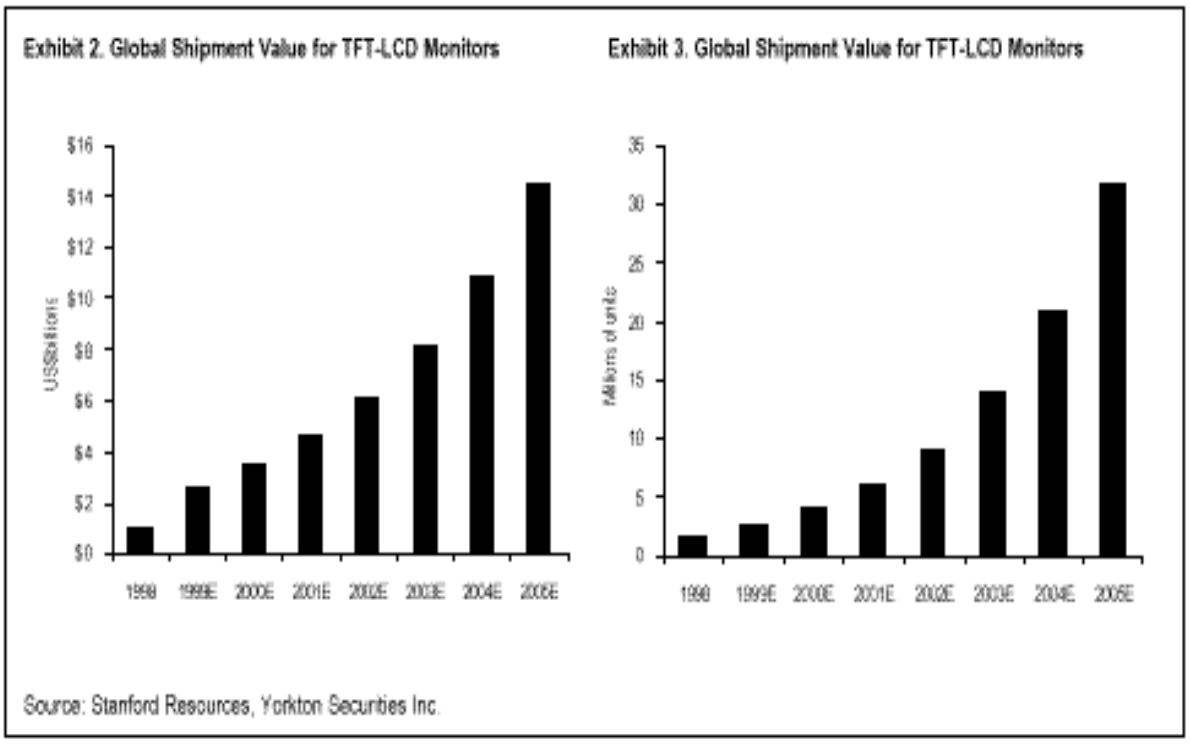
Transistor Type	Case	Operation Range	Region	$(1/2)U_PC_{OX}$	$\|V_T\|$	l
PMOS	SLOW	Vsg<0.65V	***Cut-Off*** Id=0	N/A	N/A	N/A
		Vsg>0.65V Vsd<Vsg-0.5656	***Triode*** Id=(1/2)*Up*Cox[2(Vsg-|Vt|)*Vsd-Vsd^2]	$1.10x10^{-5}$	0.5656	N/A
		Vsg>0.65V Vsd>Vsg-0.5656	***Active*** Id=(1/2)Up*Cox*(Vsg-|Vt|)^2 *(1+λ*[Vsd-Veff])	$1.10x10^{-5}$	0.5656	$1.58x10^{-2}$
	NOML	Vsg<0.65V	***Cut-Off*** Id=0	N/A	N/A	N/A
		Vsg>0.65V Vsd<Vsg-0.5856	***Triode*** Id=(1/2)*Up*Cox[2(Vsg-|Vt|)*Vsd-Vsd^2]	$1.505x10^{-5}$	0.5856	N/A
		Vsg>0.65V Vsd>Vsg-0.5856	***Active*** Id=(1/2)Up*Cox*(Vsg-|Vt|)^2 *(1+λ*[Vsd-Veff])	$1.505x10^{-5}$	0.5856	$1.49x10^{-2}$
	FAST	Vsg<0.65V	***Cut-Off*** Id=0	N/A	N/A	N/A
		Vsg>0.65V Vsd<Vsg-0.5442	***Triode*** Id=(1/2)*Up*Cox[2(Vsg-|Vt|)*Vsd-Vsd^2]	$1.734x10^{-5}$	0.544	N/A
		Vsg>0.65V Vsd>Vsg-0.5442	***Active*** Id=(1/2)Up*Cox*(Vsg-|Vt|)^2 *(1+λ*[Vsd-Veff])	$1.734x10^{-5}$	0.544	$1.68x10^{-2}$

The following graphs demonstrate the accuracy of the square-law current-voltage model with Hspice simulation for various transistor gate lengths and widths. For the I_D vs. V_{GS} plots, all currents are normalised with respect to geometrical dimension (i.e. the current plotted is I_Dx(L/W), where L and W are the gate lengths and widths of the transistor respectively). The analytical expressions for I_D vs. V_{DS} were also obtained and verified for various gate-source voltages and various transistor sizes. However, to remain brief, only the I_D-V_{DS} relationship for a transistor with a gate length of 1um and width of 10um is shown for multiple gate-source voltages. As well, only slow case comparisons are demonstrated.

Appendix 4:

Predicted Growth Trend for the Flat Panel Industry

Graph 1: Predicted Market growth for FPDs (Stanford Resources Market Research)



Appendix 5:

Gantt Timetable for the Proposed PLL

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